

Vegas Schematic

SKL/KBL-U

2016/06/27

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Core Design>



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Cover Page

Size
A4

Document Number

Vegas SKL/KBL-U

Rev

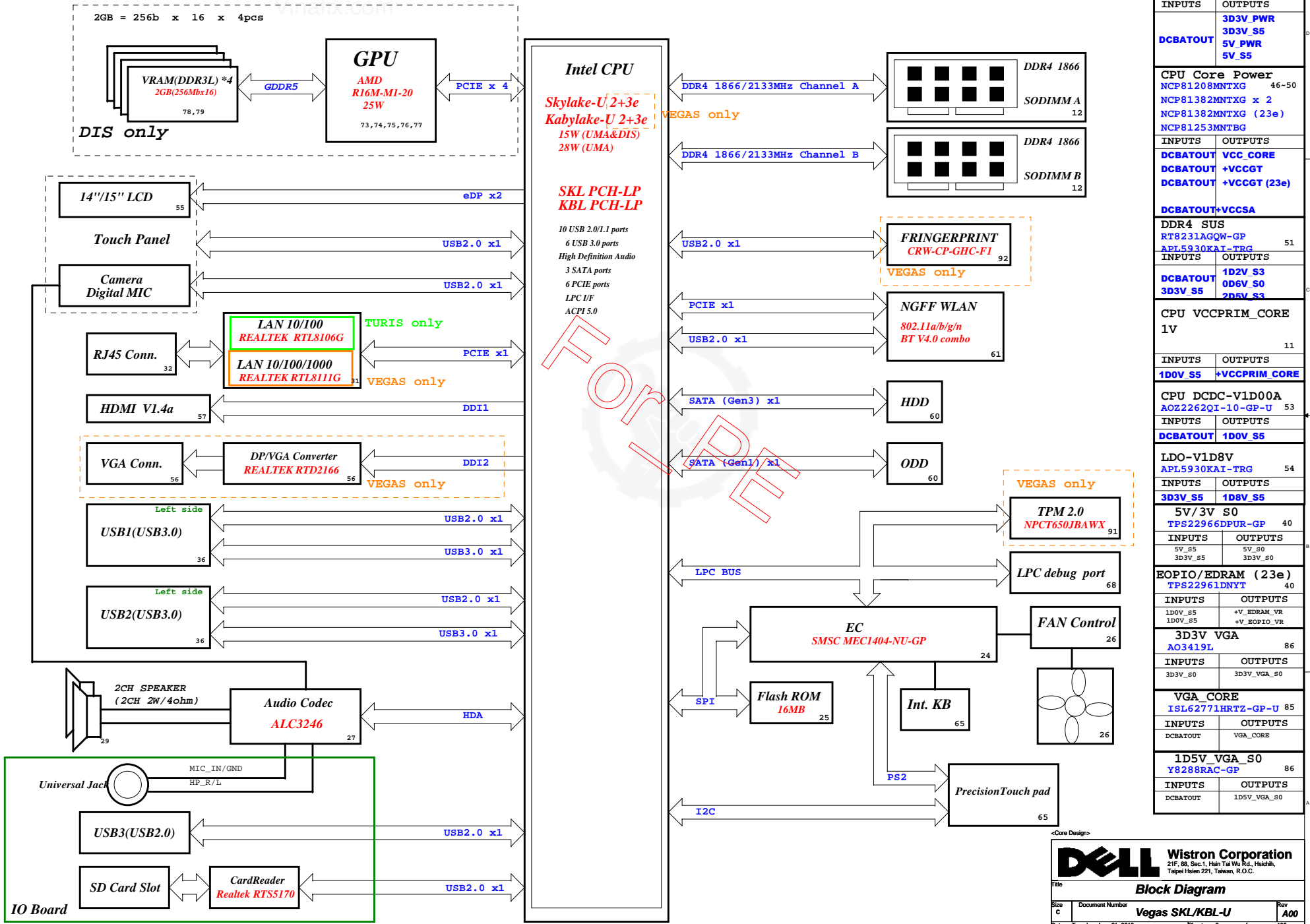
A00

Date: Monday, June 27, 2016

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Project code:4PD09P010001
PCB P/N: 15341-SD
Revision: A00


Vegas SKL-U/KBL-U Block Diagram



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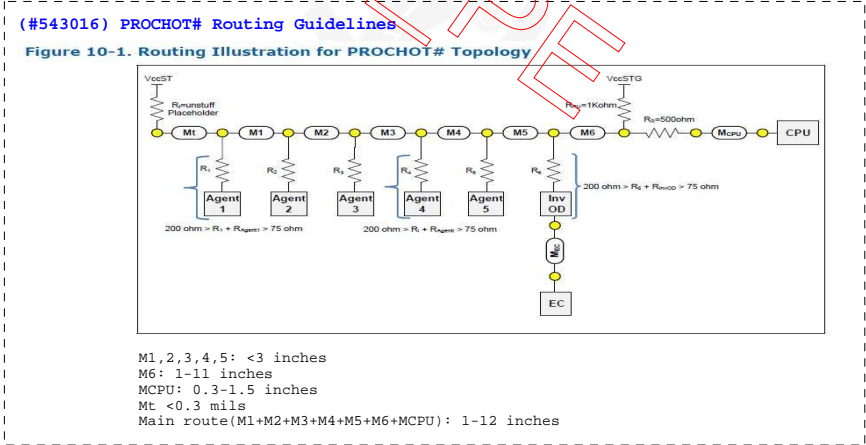
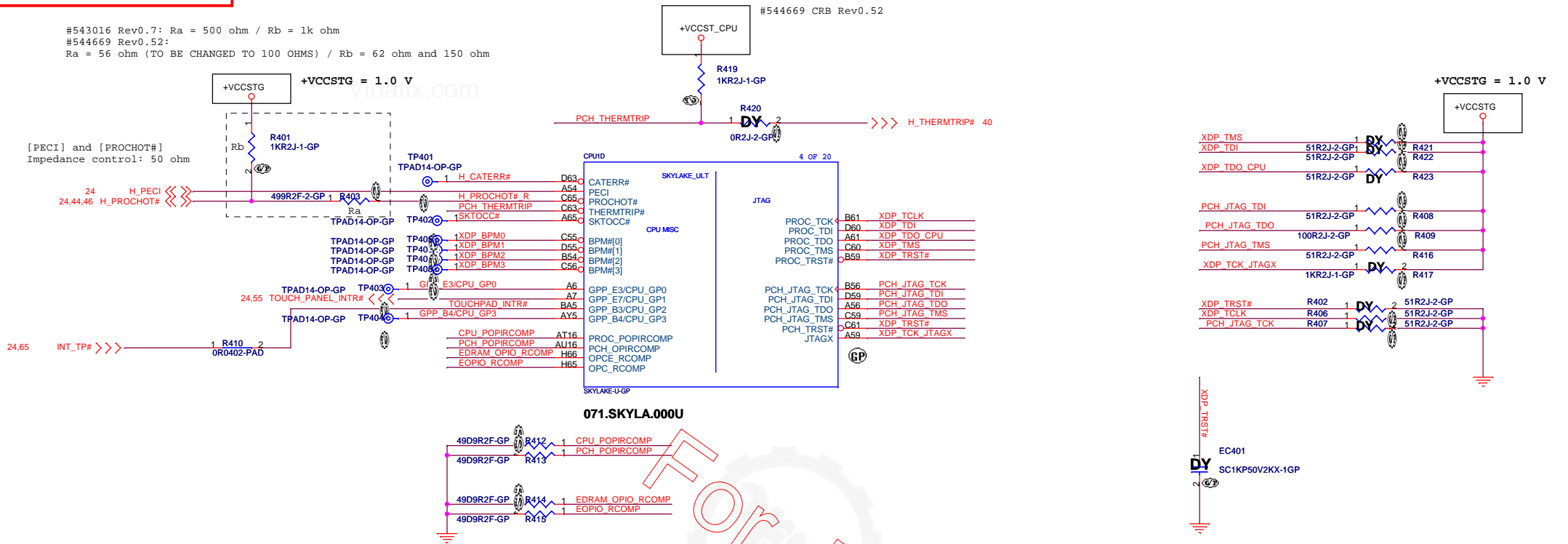


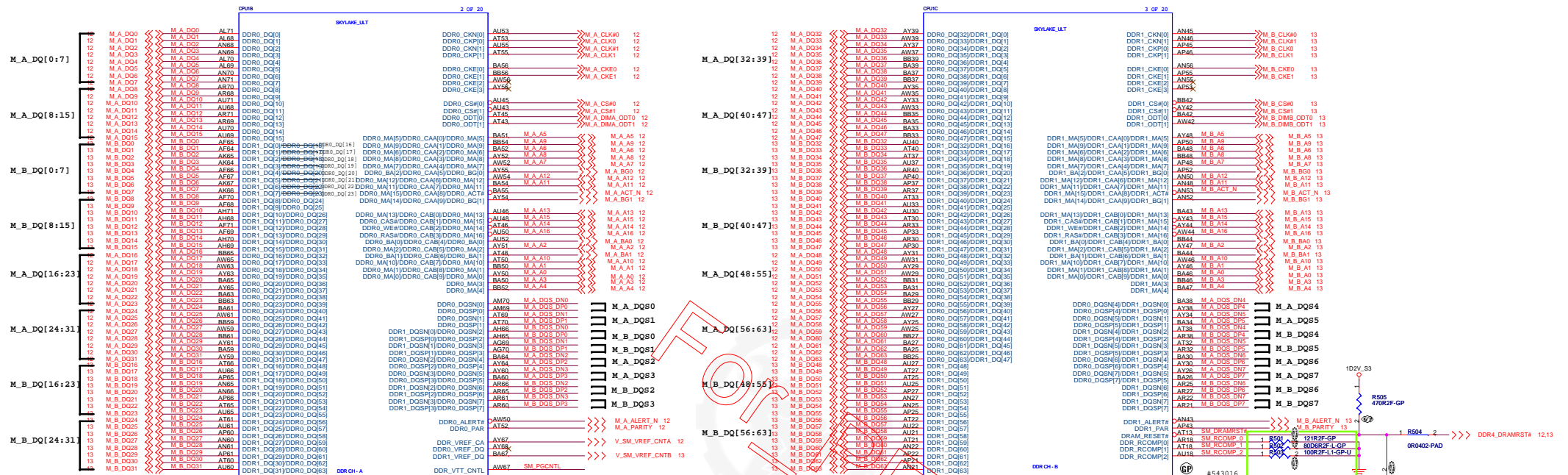
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Main Func = CPU

#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm





071.SKYLA.000U

071.SKYLA.000U

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

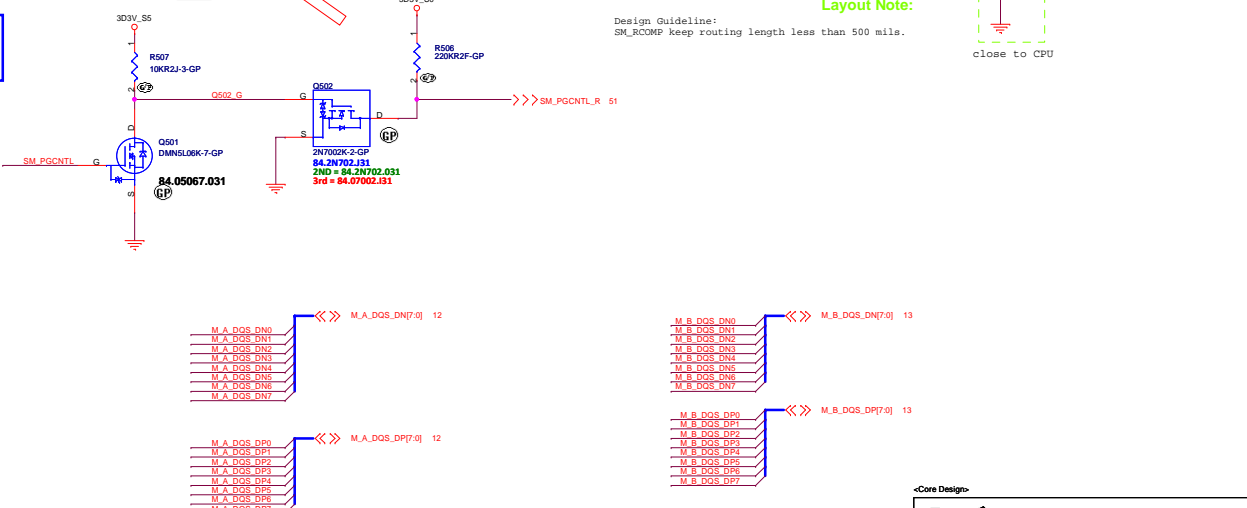
4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory Type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processors	DDR0_ODT[0] (DRL_ODT[0])	Processor's ODT[0] connected to DIMM/Rank0 ODT. Topology connection	1,2
			One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processors	DDR0_ODT[1:0] (DRL_ODT[1:0])	Processor's ODT[0] connected to DIMM/Rank0 ODT. Topology connection	1,2
			One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
DDR3L Memory Down	Processors	Processors	DDR0_ODT[0] (DRL_ODT[0])	Processor's ODT[0] connected to DIMM/Rank0 ODT	3,4
			One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
DDR3L SO-DIMM	Processors	Processors	DDR0_ODT[1:0] (DRL_ODT[1:0])	Processor's ODT[0] connected to DIMM/Rank0 ODT	1,3
			One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
DDR3L Mixed Memory SO-DIMM	Processors	Processors	DDR0_ODT[1:0] (DRL_ODT[1:0])	Processor's ODT[0] connected to DIMM/Rank0 ODT	3,4
			One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
DDR4 Memory Down	Processors	Processors	DDR0_ODT[0] (DRL_ODT[0])	Processor's ODT[0] connected to DIMM/Rank0 ODT	3,4
			One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
DDR4 SO-DIMM	Processors	Processors	DDR0_ODT[1:0] (DRL_ODT[1:0])	Processor's ODT[0] connected to DIMM/Rank0 ODT	1,3
			One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		

Notes:

- For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (VDFP - Intel LPDDR3, VDFP - Intel LPDDR3, VDFP - Intel LPDDR3).
- DDR3L ODT input is used high (Active). RTT_NOM is defined by BIOS as high/2 in both ranks, when a Rank receives write command it enables RTT_NOM (set by BIOS after power training). Otherwise ODT pins are RTT_NOM (high/2).
- These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 DDP dual sided and 2R x8 dual sided.



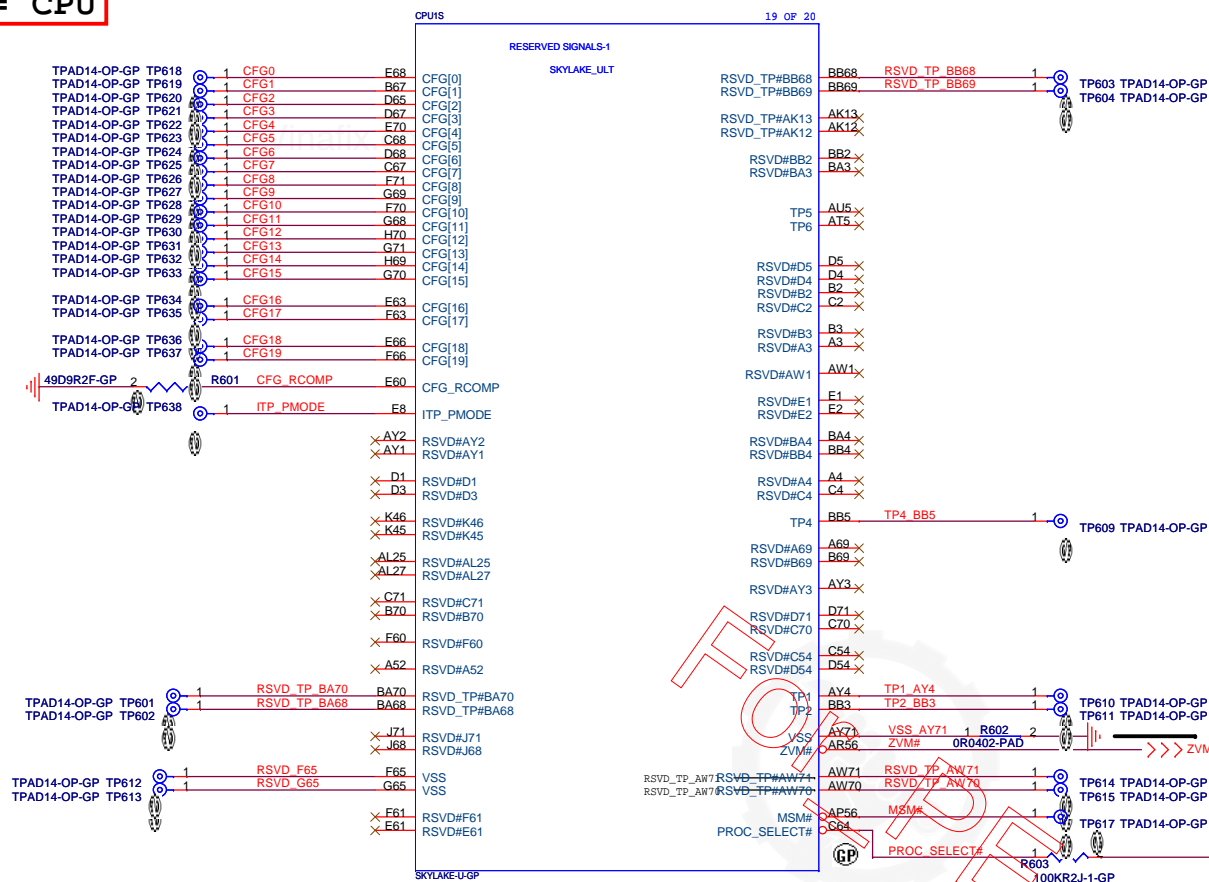
Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

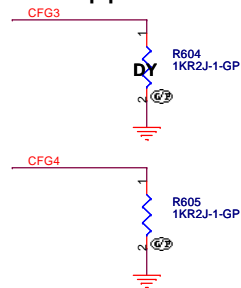
close to CPU

-Core Design-

Main Func = CPU



PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX_ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG TERMINATIONS

#544669 Rev0.52 (CRB)

20140807 david

SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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Title

CPU (RESERVED)

Size
A3

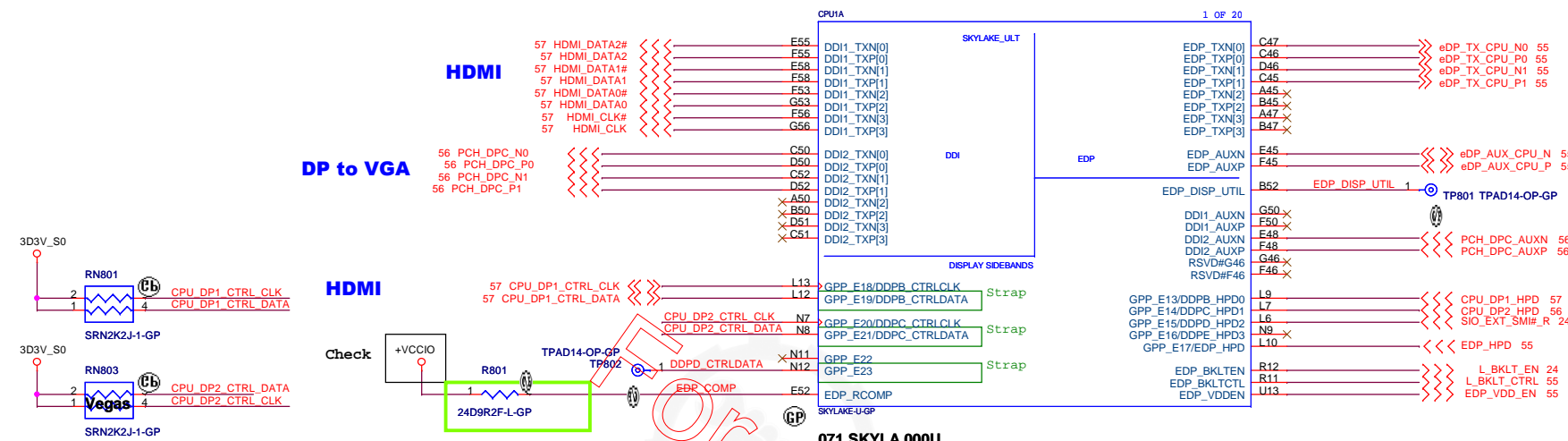
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071.SKYLA.000U
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

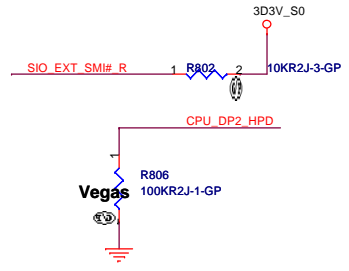
Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.


Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 $\pm 1\%$ Ω resistor.



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CORE

U-line 23e 28W
IccMax current-10ms max = 34 A

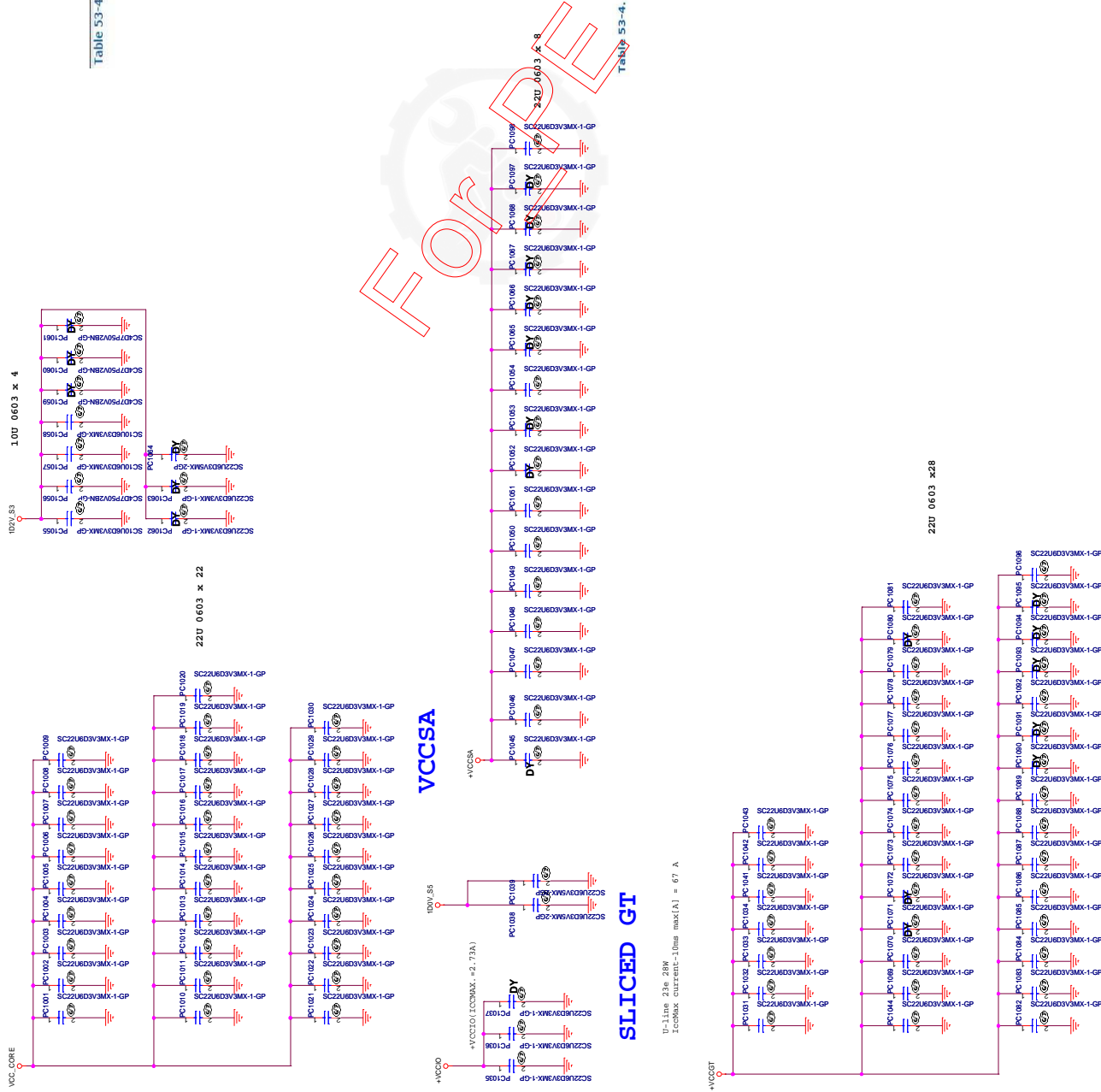


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (0.4-5mΩ ESR)	Placed at primary side near to VR output
VCC Power Plane at VR output	1x 220uF (0.4-5mΩ ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (0.4-5mΩ ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (0.4-5mΩ ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGT Power Plane at VR output	1x 220uF (0.4-5mΩ ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0005	Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47uF 0005	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
VCCGT		8x 47uF 0905 (6.3V)	Place as close to the package as possible
		8x 10uF 0402	
	10x 10uF 0402 12x 1uF 0201		Place on secondary side, underneath the package
VCCGTx		3x 47uF 0905 (6.3V) ¹	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0905	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
VCCSA		8x 22uF 0603	Place on secondary side, underneath the package
	7x 10uF 0402 7x 1uF 0201		
VCCIO		6x 10uF 0402	Place as close to the package as possible
	2x 10uF 0402 4x 1uF 0201		Place on secondary side, underneath the package
VDDQ	2x 10uF 0402 4x 1uF 0201	4x 1uF 0402	Place as close to the package as possible
			Place on secondary side, underneath the package
VDDQC			
	1x 1uF 0201	4x 10uF 0402	Place as close to the package as possible
VCCPLL		1x 1uF 0402	Place on secondary side, underneath the package
	VCCST		Place as close to the package as possible

Table 53-4.

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Facelider only
VCCDEPIO	2x: 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x: 10uF 0402 6x: 1uF 0201		Place on secondary side, underneath the package

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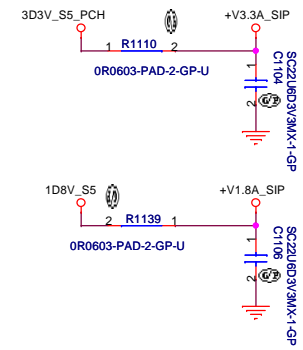
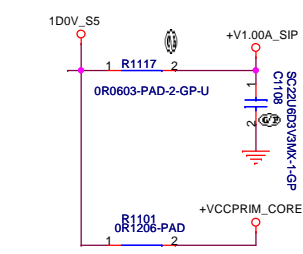


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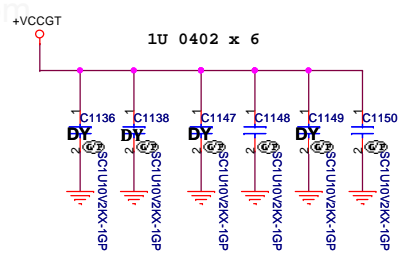
CPU (Power CAP1)

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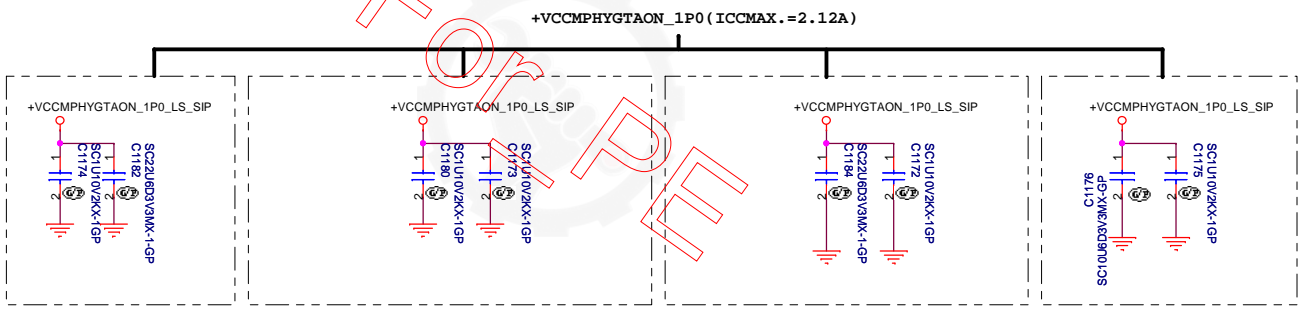
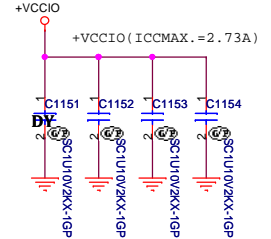
PCH DERIVED RAILS



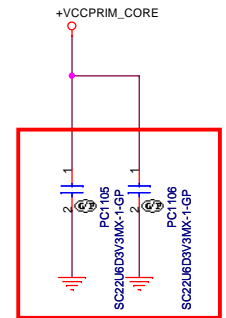
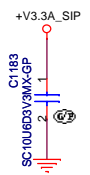
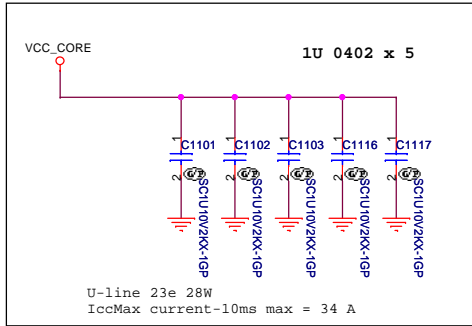
UNSLICED GT



VCCIO



Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15



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For P/E

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Main Func = PCH

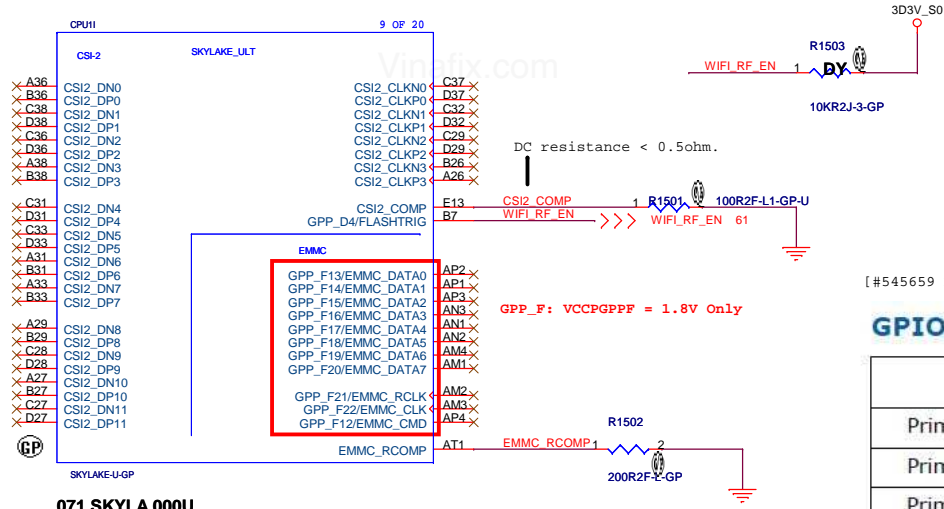


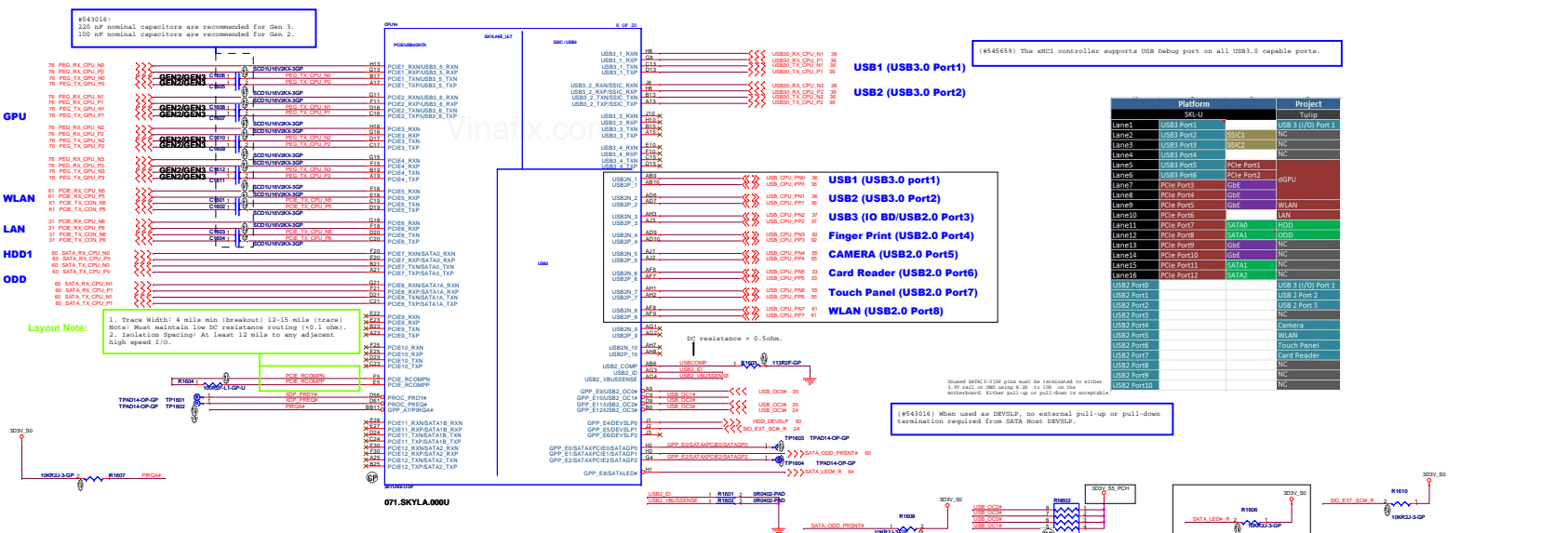
Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



Platform		Project
	Str-U	Tulip
Line#1	USB#0 Port1	USB 1 (V) Port 1
Line#2	USB#0 Port2	SSC1
Line#3	USB#0 Port3	SSC2
Line#4	USB#0 Port4	NC
Line#5	USB#0 Port5	PCIe Port1
Line#6	USB#0 Port6	PCIe Port2
Line#7	PCIe Port1	GPIO
Line#8	PCIe Port2	GPIO
Line#9	PCIe Port3	GPIO
Line#10	PCIe Port4	GPIO
Line#11	PCIe Port7	SATA0
Line#12	PCIe Port8	SATA1
Line#13	PCIe Port9	GPIO
Line#14	PCIe Port10	GPIO
Line#15	PCIe Port11	SATA2
Line#16	PCIe Port12	SATA2
USB#0 Port0		USB 1 (V) Port 1
USB#0 Port1		USB 1 Port 2
USB#0 Port2		USB 1 Port 3
USB#0 Port3		NC
USB#0 Port4		Camera
USB#0 Port5		WLAN
USB#0 Port6		Touch Panel
USB#0 Port7		Card Reader
USB#0 Port8		NC
USB#0 Port9		NC
USB#0 Port10		NC

PCIe Table			USB 2.0 Table	
Port	Device	Share BUS	Pair	Device
1	N/A	USB3_0_3	0	USB3.0 port1
2	N/A	USB3_0_4	1	USB3.0 port2
3	WLAN		2	USB2.0 Port3 (IOBD)
4	LAN		3	Finger Print
5(L0-L3)	GPU		4	CAMERA
6(L3)	HDD	SATA0	5	Card Reader
6(L2)	ODD	SATA1	6	Touch Panel
6(L0-L1)	N/A		7	WLAN

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

1	PCle #12	SATA #2	X4	X2	Intel PCIe Storage Device #3
2	PCle #11	SATA #1			
3	PCle #10	GbE	X4	X2	Intel PCIe Storage Device #3
4	PCle #9	GbE			
5	PCle #8	SATA #1	X2	X2	Intel PCIe Storage Device #2
6	PCle #7	SATA #0			
7	PCle #6	GbE	X2	X2	Intel PCIe Storage Device #2
8	PCle #5	GbE			
9	PCle #4	GbE	X2	X2	Intel PCIe Storage Device #1
10	PCle #3	GbE			
11	PCle #2	X4	X2	X2	Intel PCIe Storage Device #1
12	PCle #1				
13	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
14	PCle #4				
15	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
16	PCle #2				
17	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
18	PCle #0				
19	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
20	PCle #4				
21	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
22	PCle #2				
23	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
24	PCle #0				
25	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
26	PCle #4				
27	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
28	PCle #2				
29	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
30	PCle #0				
31	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
32	PCle #4				
33	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
34	PCle #2				
35	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
36	PCle #0				
37	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
38	PCle #4				
39	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
40	PCle #2				
41	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
42	PCle #0				
43	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
44	PCle #4				
45	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
46	PCle #2				
47	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
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57	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
58	PCle #2				
59	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
60	PCle #0				
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63	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
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65	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
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85	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
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87	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
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89	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
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103	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
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118	PCle #2				
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120	PCle #0				
121	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
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123	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
124	PCle #2				
125	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
126	PCle #0				
127	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
128	PCle #4				
129	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
130	PCle #2				
131	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
132	PCle #0				
133	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
134	PCle #4				
135	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
136	PCle #2				
137	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
138	PCle #0				
139	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
140	PCle #4				
141	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
142	PCle #2				
143	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
144	PCle #0				
145	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
146	PCle #4				
147	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
148	PCle #2				
149	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
150	PCle #0				
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152	PCle #4				
153	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
154	PCle #2				
155	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
156	PCle #0				
157	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
158	PCle #4				
159	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
160	PCle #2				
161	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
162	PCle #0				
163	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
164	PCle #4				
165	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
166	PCle #2				
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169	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
170	PCle #4				
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172	PCle #2				
173	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
174	PCle #0				
175	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
176	PCle #4				
177	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
178	PCle #2				
179	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
180	PCle #0				
181	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
182	PCle #4				
183	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
184	PCle #2				
185	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
186	PCle #0				
187	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
188	PCle #4				
189	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
190	PCle #2				
191	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
192	PCle #0				
193	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
194	PCle #4				
195	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
196	PCle #2				
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198	PCle #0				
199	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
200	PCle #4				
201	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
202	PCle #2				
203	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
204	PCle #0				
205	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
206	PCle #4				
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208	PCle #2				
209	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
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213	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
214	PCle #2				
215	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
216	PCle #0				
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222	PCle #0				
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260	PCle #4				
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262	PCle #2				
263	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
264	PCle #0				
265	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
266	PCle #4				
267	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
268	PCle #2				
269	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
270	PCle #0				
271	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
272	PCle #4				
273	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
274	PCle #2				
275	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
276	PCle #0				
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278	PCle #4				
279	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
280	PCle #2				
281	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
282	PCle #0				
283	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
284	PCle #4				
285	PCle #3	X4	X2	X2	Intel PCIe Storage Device #1
286	PCle #2				
287	PCle #1	X4	X2	X2	Intel PCIe Storage Device #1
288	PCle #0				
289	PCle #5	X4	X2	X2	Intel PCIe Storage Device #1
290	PCle				

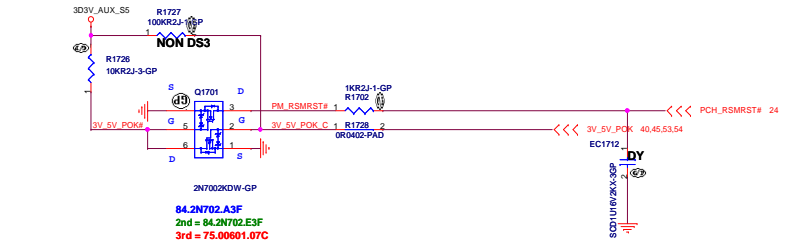
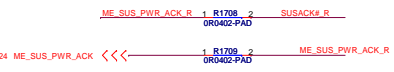
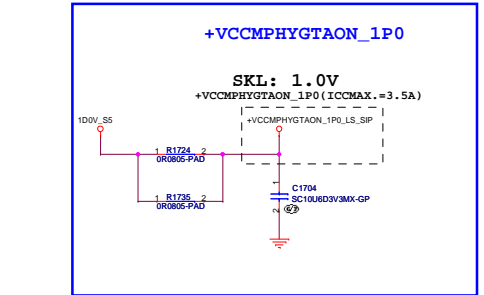
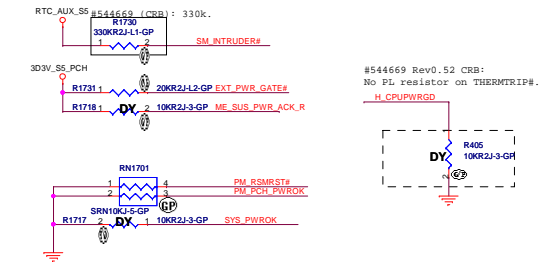
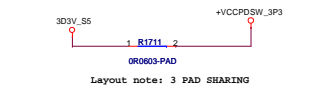
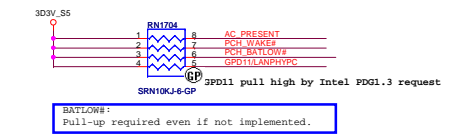
Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

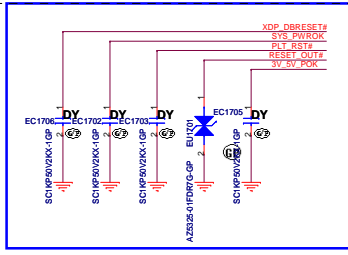
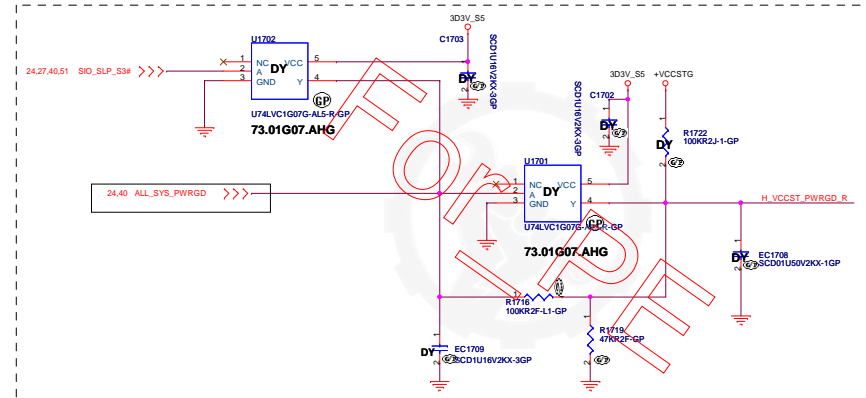
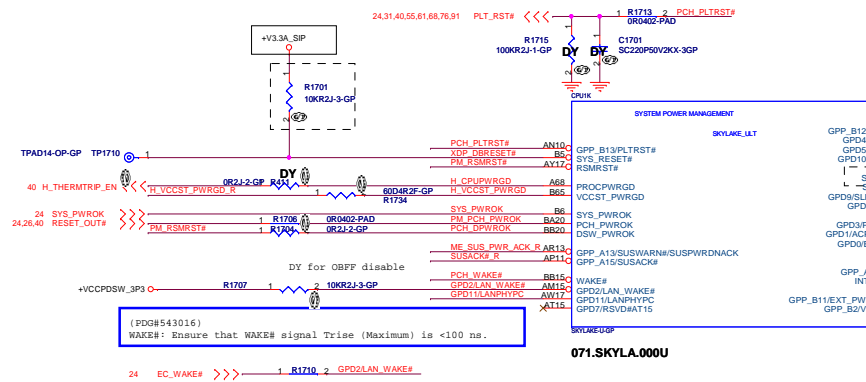
Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe-Link Config	PCI Express [®] Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
	1x4	Port1				Port5				Port9			
Y	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9		Port10	

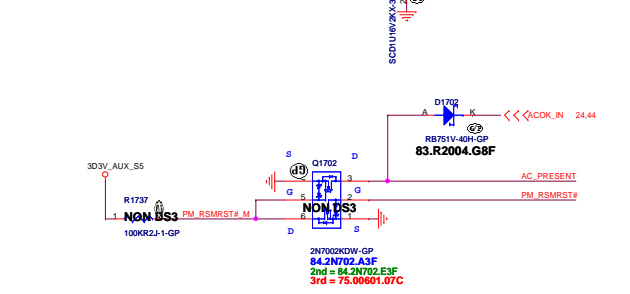
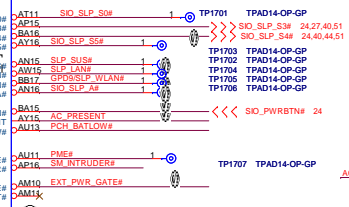
Main Func = PCH



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1843016 Rev0.7
EXT_PWR_GATE# Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 25k pull-down that is active during the early portion of the power up sequence



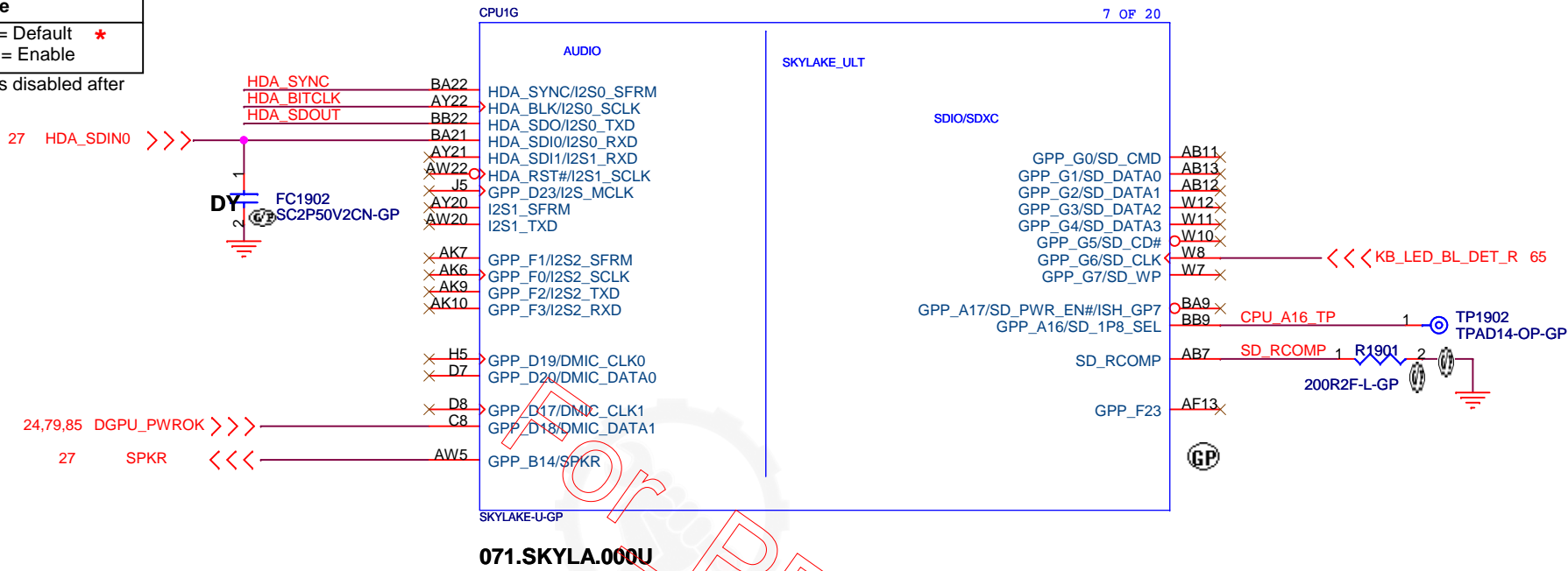
#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during 6x pwr states, regardless of the voltage level of VCCST

Main Func = PCH

PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

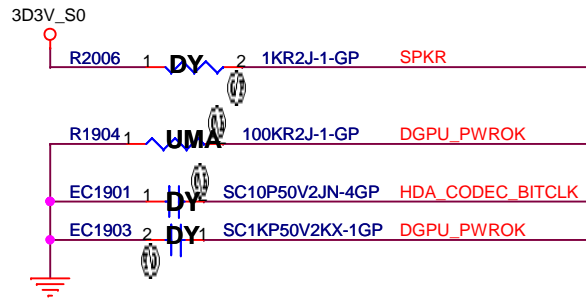


071.SKYLA.000U

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



27 HDA_CODEC_BITCLK <<< 1 R1907 2 0R0402-PAD HDA_BITCLK
27 HDA_CODEC_SYNC <<< 1 R1908 2 0R0402-PAD HDA_SYNC

27 HDA_CODEC_SDOUT <<< 1 R1912 2 0R0402-PAD HDA_SDOUT
24 ME_FWP_EC <<< R1909 1 1KR2J-1-GP



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (AUDIO/SDIO/SDXC)

Size A4

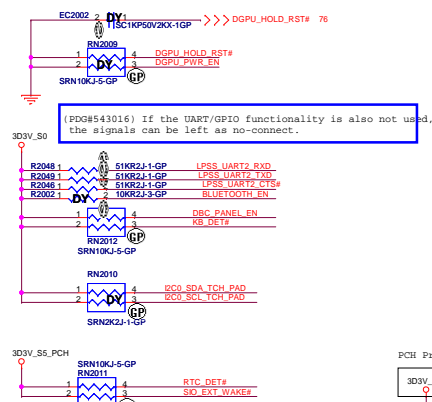
Document Number

Vegas SKL/KBL-U

Rev A00

Date: Monday, June 27, 2016

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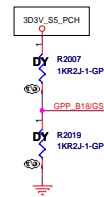


PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWRON
GSP0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITPXDP.

The signal has a weak internal pull-down.

PCH Prim



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55 DBC_PANEL_EN <<<

61 BLUETOOTH_EN <<<

24 SIO_EXT_WAKE# >>>

PTP 65 I2C0_SDA_TCH_PAD

65 I2C0_SCL_TCH_PAD

CPU/F

LPSS

SKYLAKE_ULI

ISH

6 OF 20

GPP_B15/GSP0_CS#

GPP_B16/GSP0_CLK

GPP_B17/GSP0_MISO

GPP_B18/GSP0_MOSI

GPP_B19/GSP1_CS#

GPP_B20/GSP1_CLK

GPP_B21/GSP1_MISO

GPP_B22/GSP1_MOSI

GPP_C8/UART0_RXD

GPP_C9/UART0_TXD

GPP_C10/UART0_RTS#

GPP_C11/UART0_CTS#

GPP_C20/UART2_RXD

GPP_C21/UART2_TXD

GPP_C22/UART2_RTS#

GPP_C23/UART2_CTS#

GPP_C16/I2C0_SDA

GPP_C17/I2C0_SCL

GPP_C18/I2C1_SDA

GPP_C19/I2C1_SCL

GPP_F4/I2C2_SDA

GPP_F5/I2C2_SCL

GPP_F6/I2C3_SDA

GPP_F7/I2C3_SCL

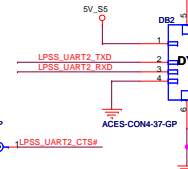
GPP_F8/I2C4_SDA

GPP_F9/I2C4_SCL

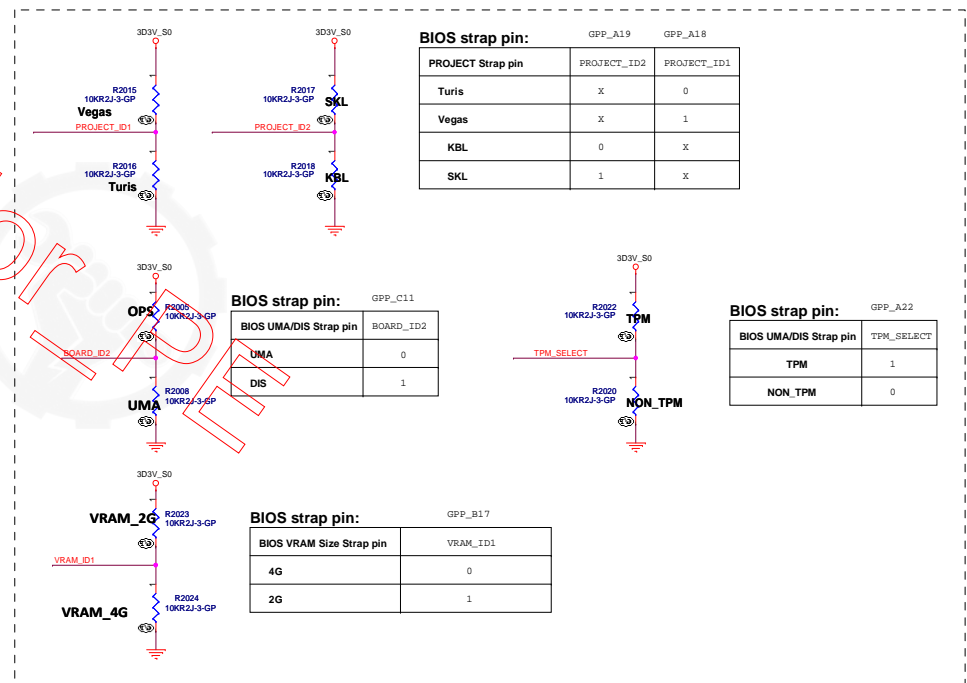
SKYLAKE_ULI

071.SKYLA.000U

For debug USB/UART:



Intel has removed ENIC controller from BOW and proposed to use UART interface for Win7 debug.



BIOS strap pin:

PROJECT Strap pin	PROJECT_ID2	PROJECT_ID1
Turis	X	0
Vegas	X	1
KBL	0	X
SKL	1	X

BIOS strap pin:

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin:

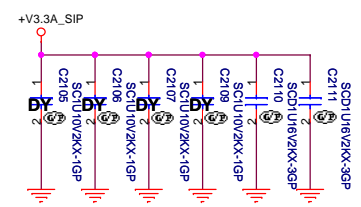
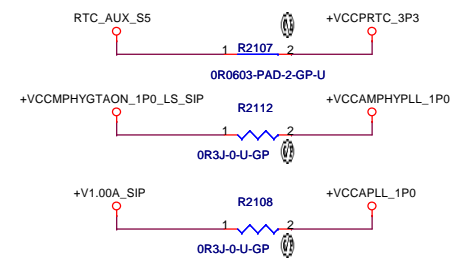
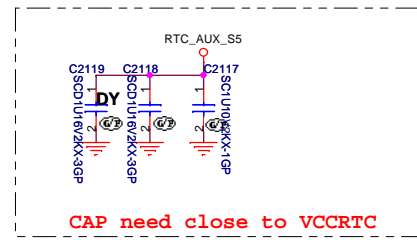
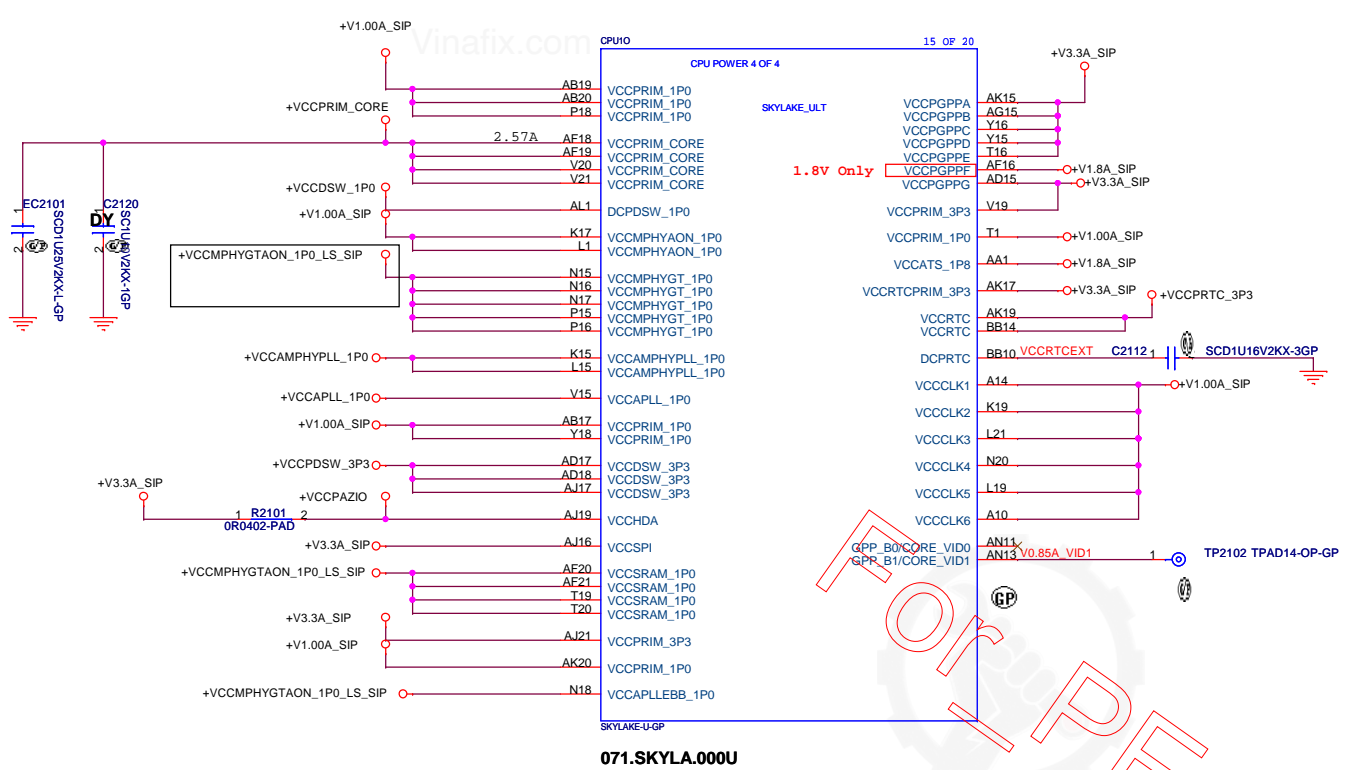
BIOS VRAM Size Strap pin	VRAM_ID1
4G	0
2G	1

BIOS strap pin:

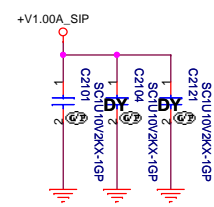
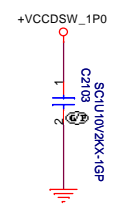
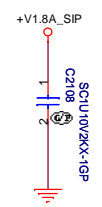
BIOS UMA/DIS Strap pin	TPM_SELECT
TPM	1
NON_TPM	0

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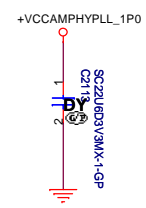
Main Func = PCH



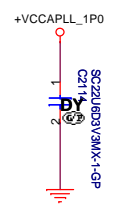
Layout Note:
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19



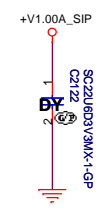
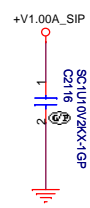
Layout Note:
1uF:
C2116 near A10
C2104 near K17
C2116 near A10
C2121 near AL1



Layout Note:
22uF:
C2113 near K15



Layout Note:
22uF:
C2113 near K15



Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

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Taipei Hsien 221, Taiwan, R.O.C.

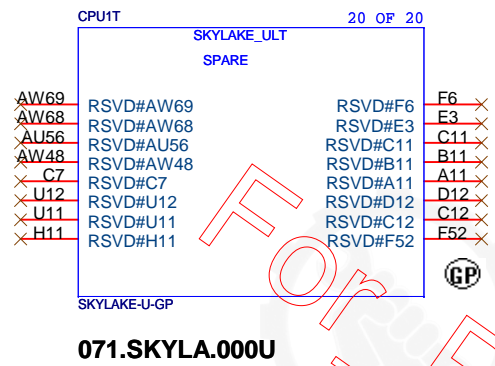
Title: **CPU (POWER1)**

Size: A3 Document Number: **Vegas SKL/KBL-U** Rev: **A00**


Date: Friday, June 24, 2016 Sheet: 21 of 105

Main Func = PCH

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (RSVD)

Size
A4

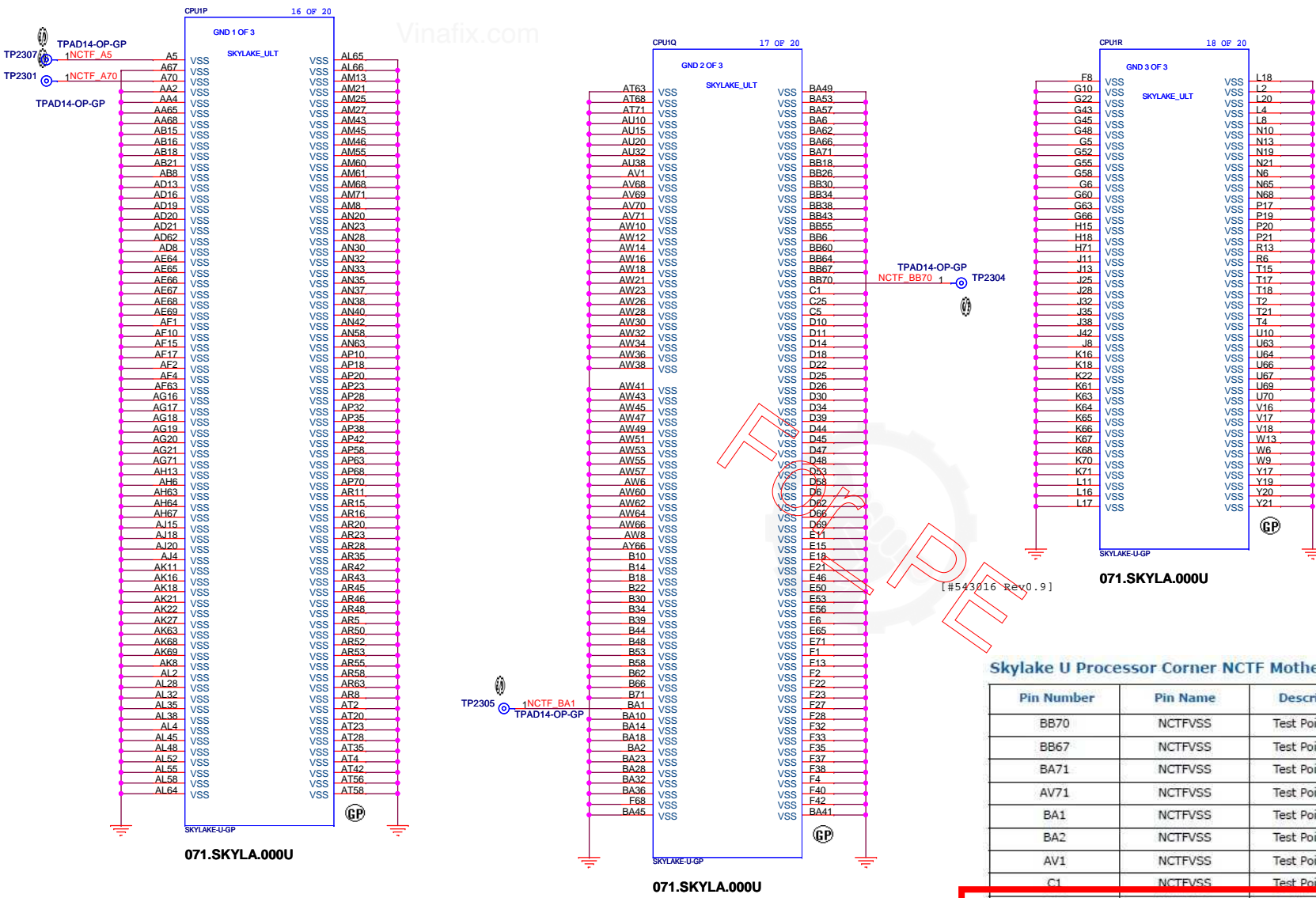
Document Number
Vegas SKL/KBL-U

Rev
A00

Date: Thursday, June 16, 2016

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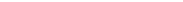
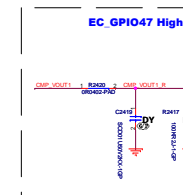
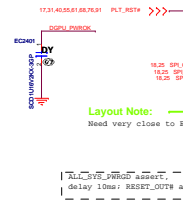
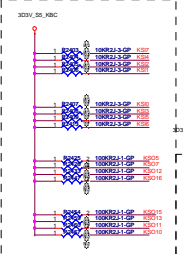
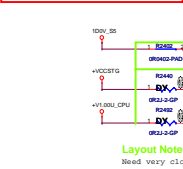
Main Func = PCH



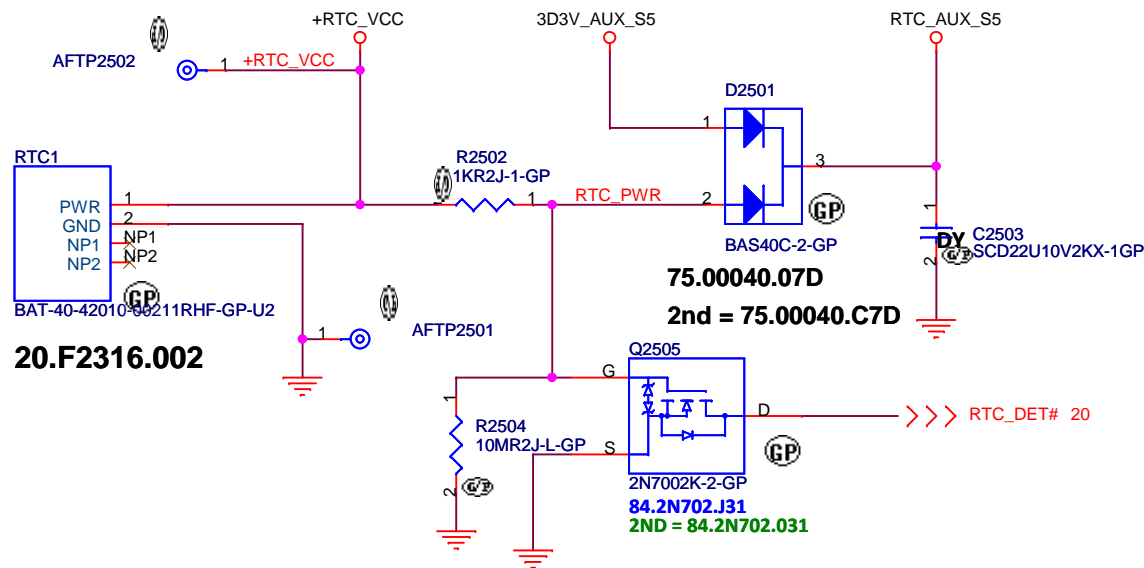
Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A71
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	Corner A71
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

Main Func = KBC



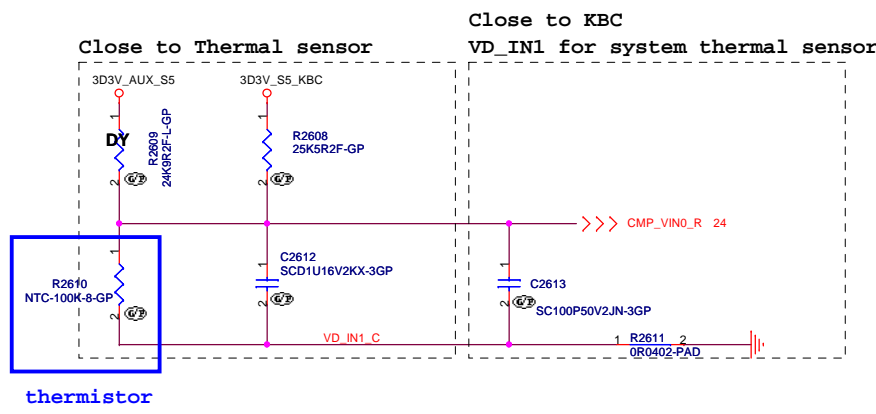
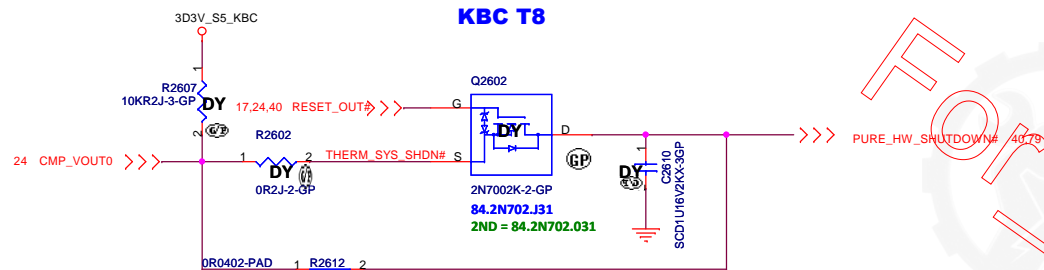
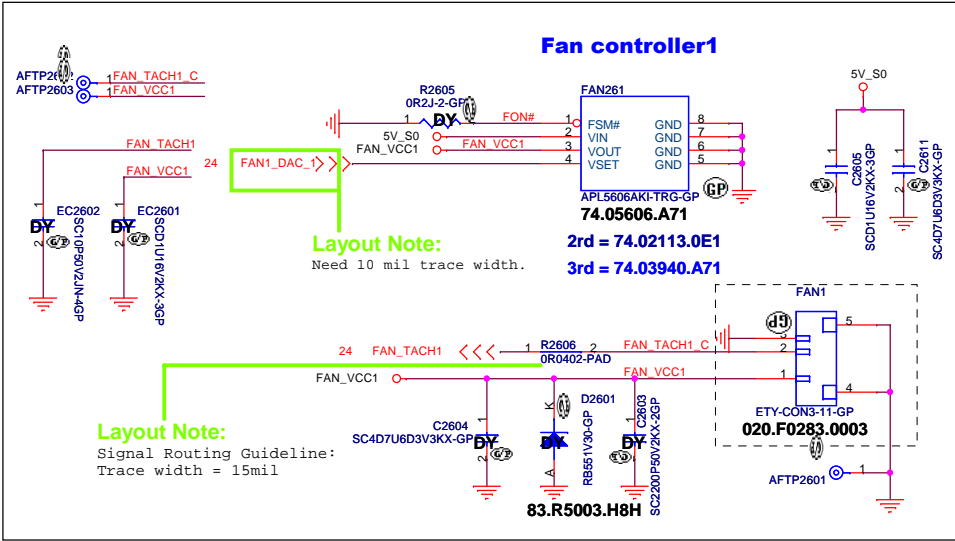
Main Func = RTC



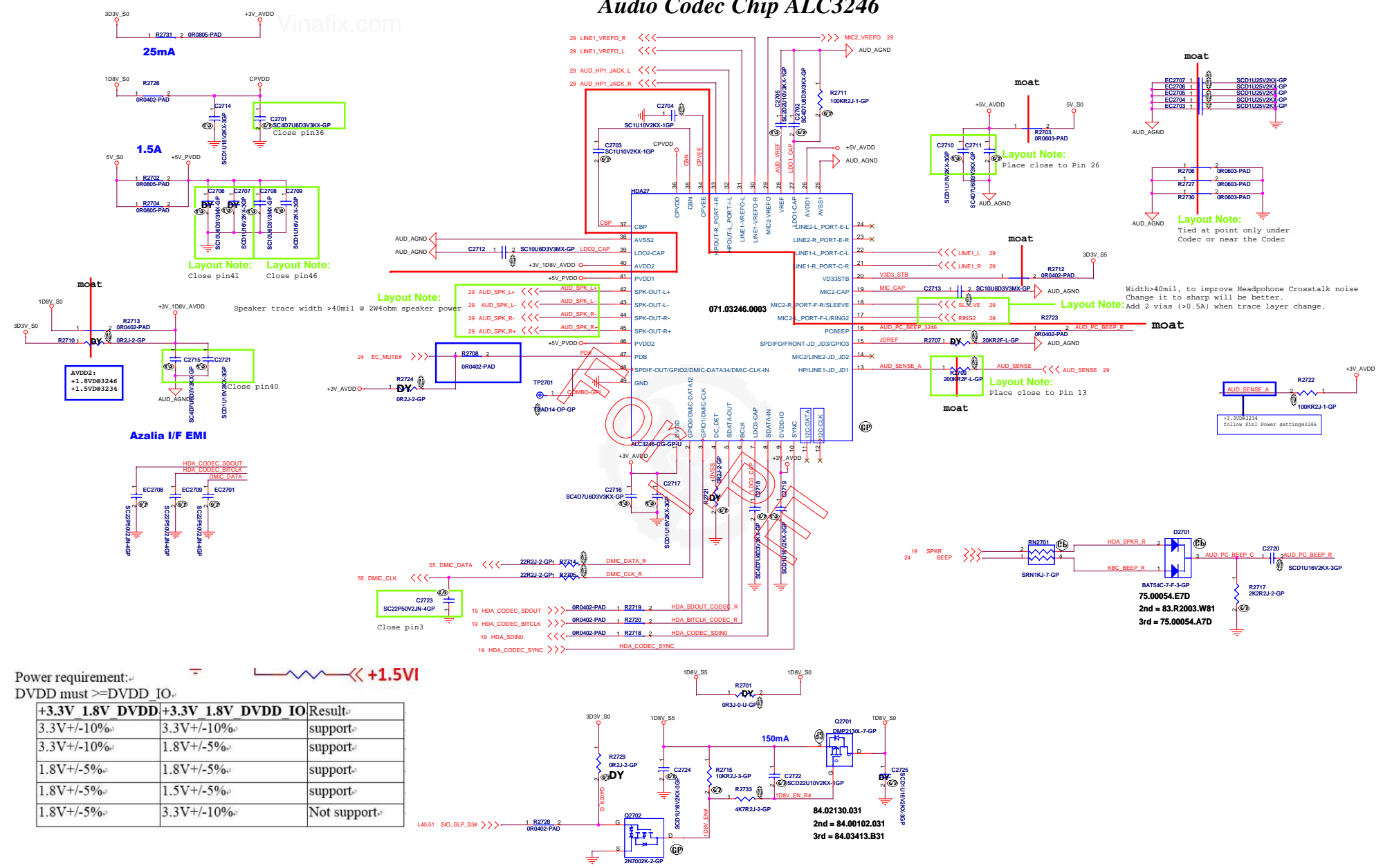
Sheet 25 of 105

Main Func = Thermal Sensor

Vinafix.com




Audio Codec Chip ALC3246



(Blanking)



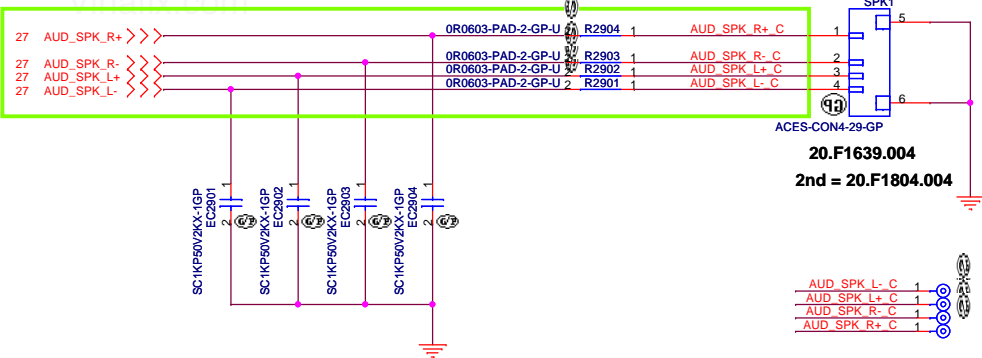
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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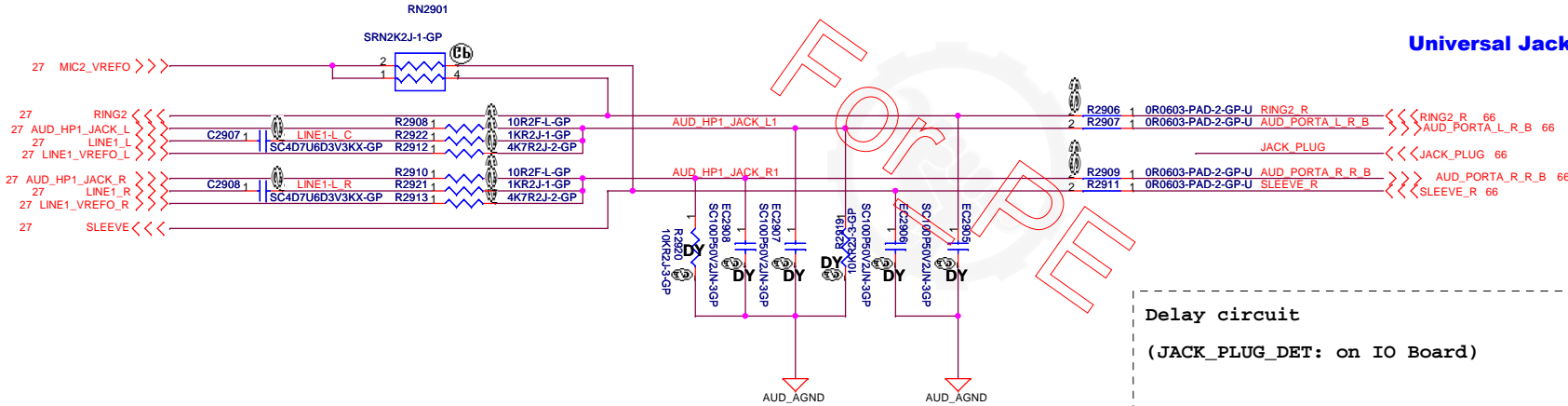
Main Func = Audio

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

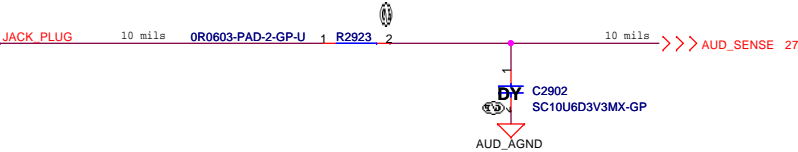


Universal Jack (Moved to I/O Board)



Delay circuit

(JACK_PLUG_DET: on IO Board)



<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Audio IO	
Size	Document Number		Rev	
A3	Vegas SKL/KBL-U		A00	
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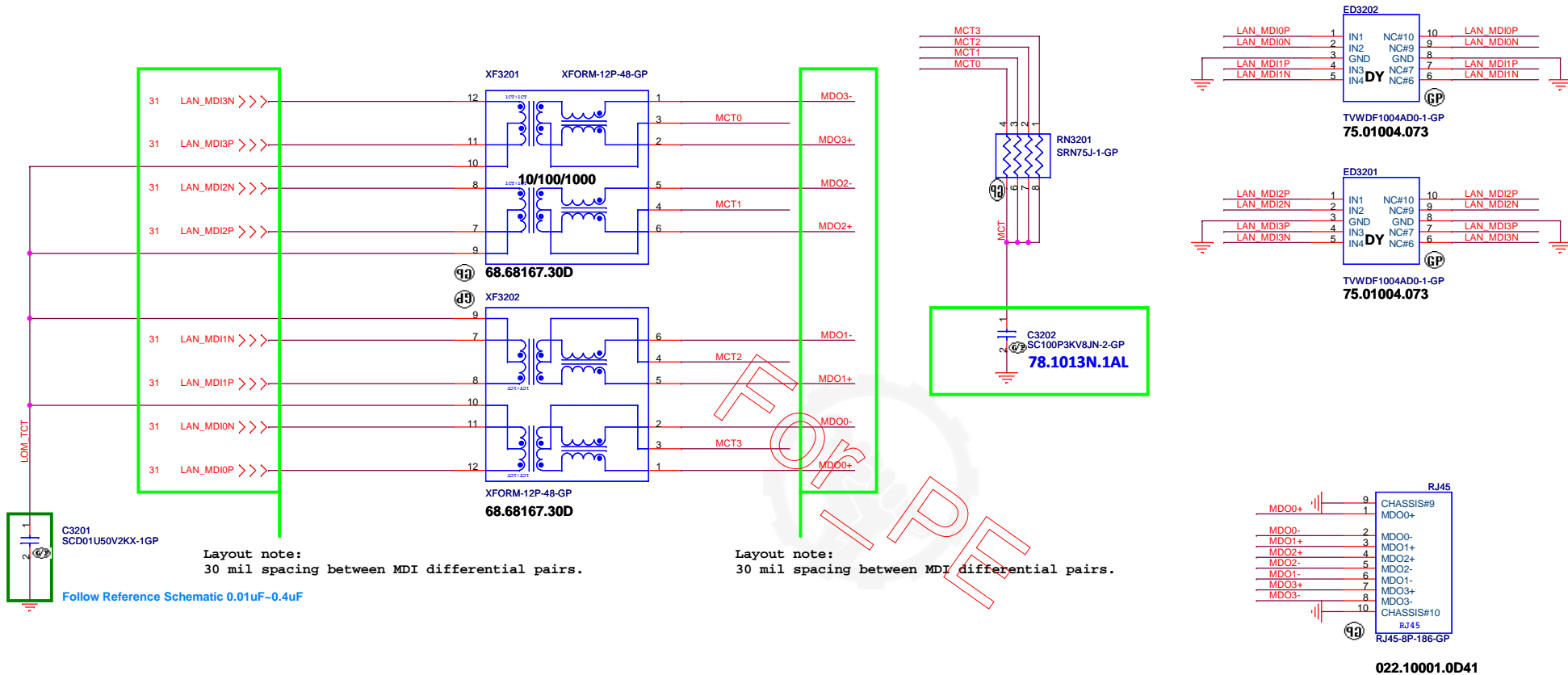
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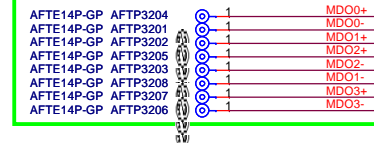
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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LAN TransFormer (10/100/1000M & 10/100M co-lay)

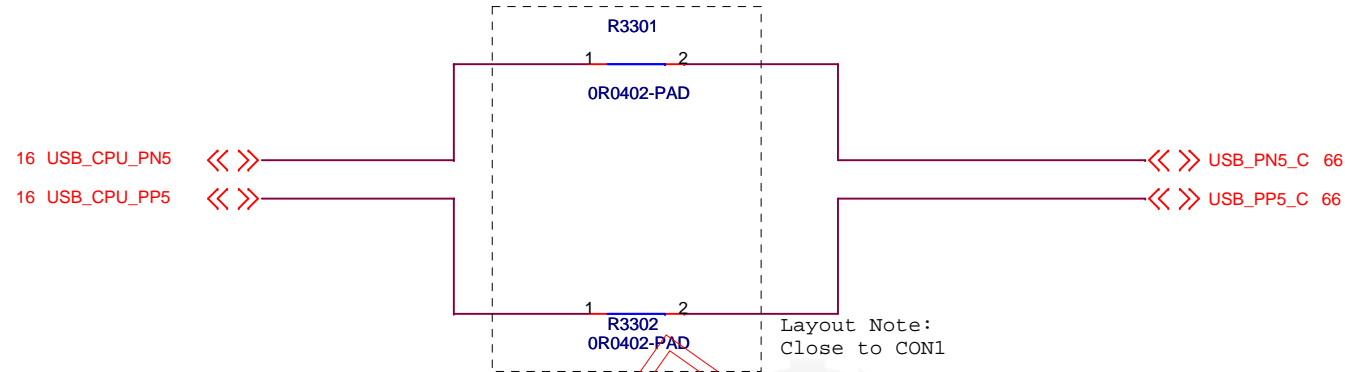


Layout:
Place near RJ45



Main Func = Card Reader

Vinafix.com



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Card Reader-RTS5170

Size
A4

Document Number

Vegas SKL/KBL-U

Rev
A00


Date: Monday, June 27, 2016

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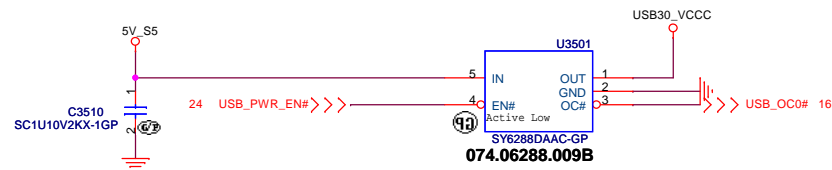
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<Core Design>

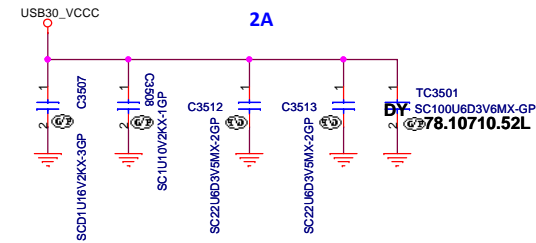
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
Date: Thursday, June 16, 2016		Sheet 34 of	105

Main Func = USB3.0 Port1

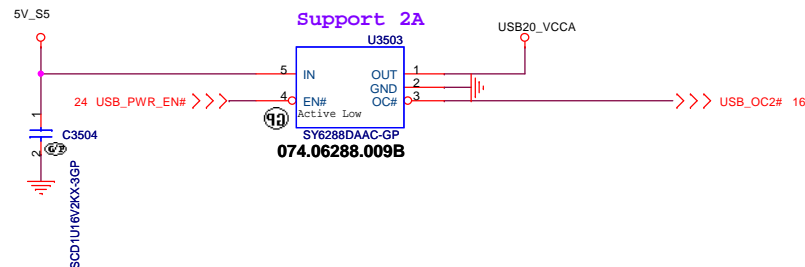


USB3.0 Port1

Layout Note: Close USB1

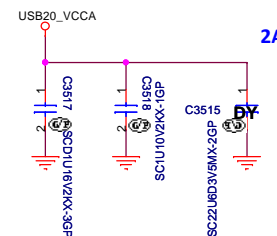


Main Func = USB2.0 Port3



USB2.0 Port3 (IO Board)

Layout Note: Close CON1



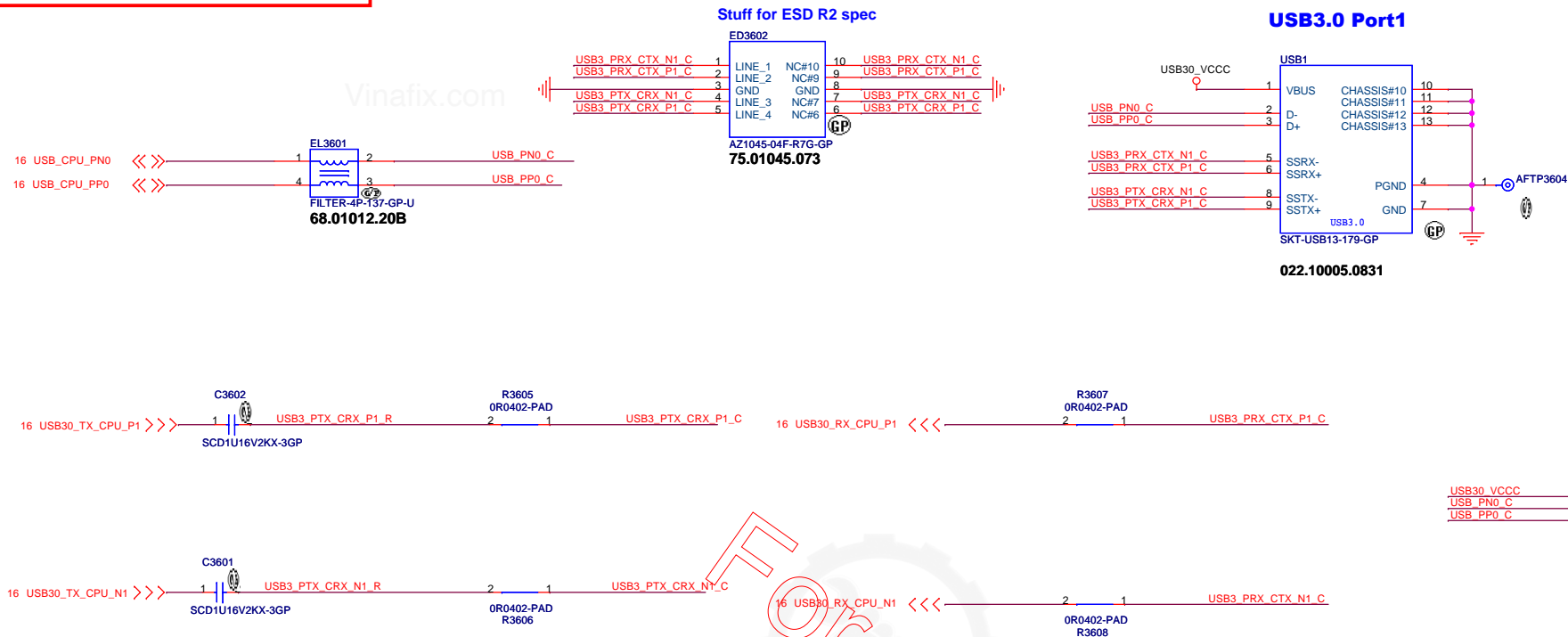
<Core Design>



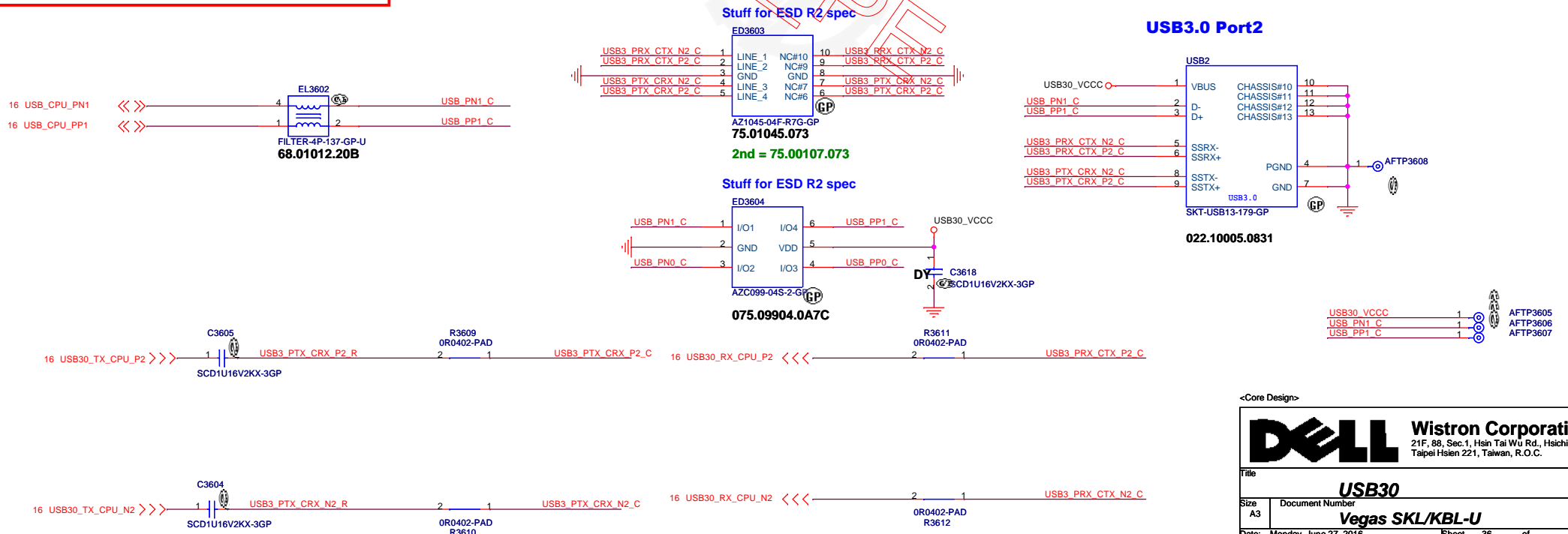
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			USB switch	
Size	Document Number	Rev		A00
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Main Func = USB3.0 Port1

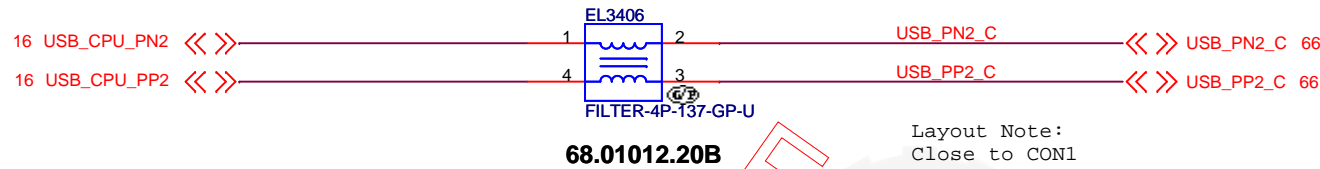


Main Func = USB3.0 Port2



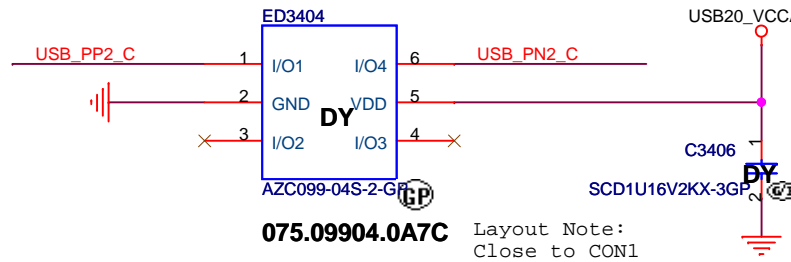
Vinafix.com

USB port 3 (USB2.0 only) CMC



USB ESD Diode

Stuff for ESD R2 spec




<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB20			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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(Blanking)

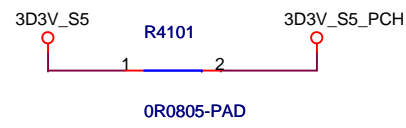


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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Main Func = Power & Sequence

Vinafix.com



For PFE


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Connected_Standby(1/2)+DS3		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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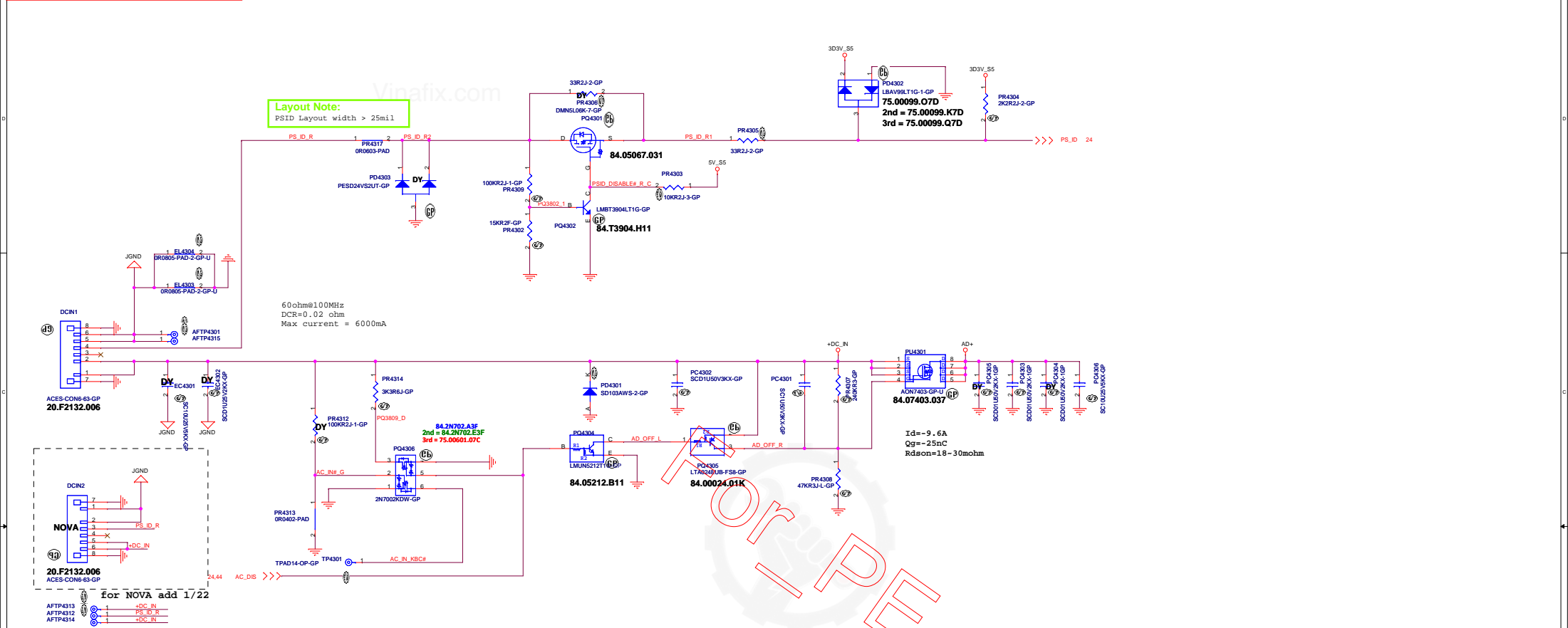
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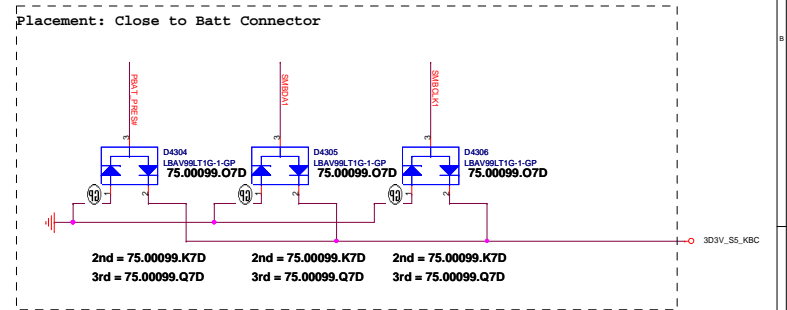
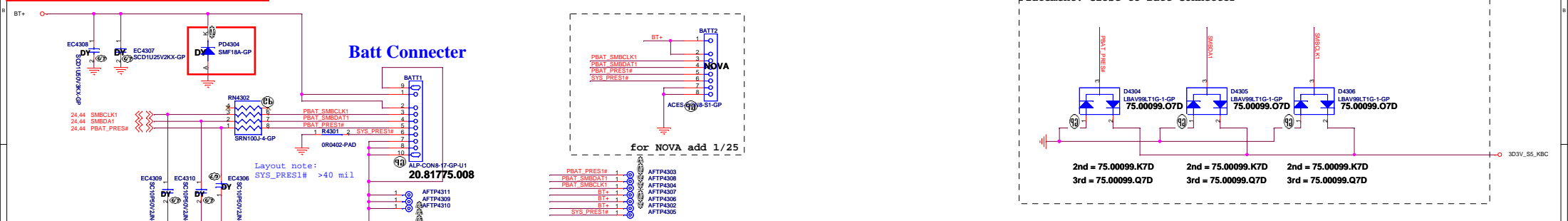
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Connected_Standby(2/2)		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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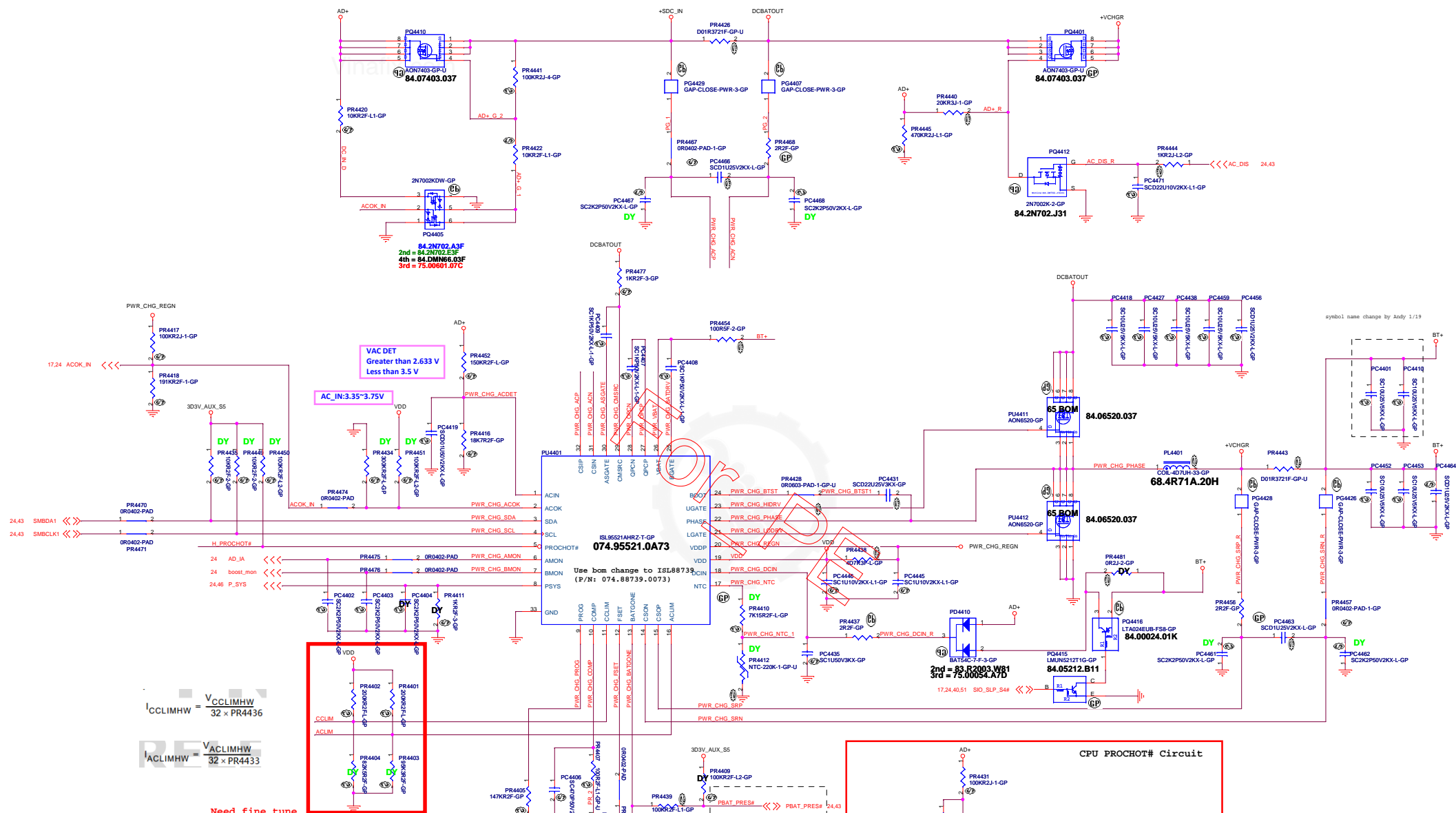
Main Func = ADT Input



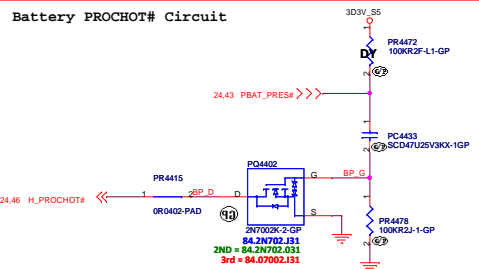
Main Func = M-BAT Input



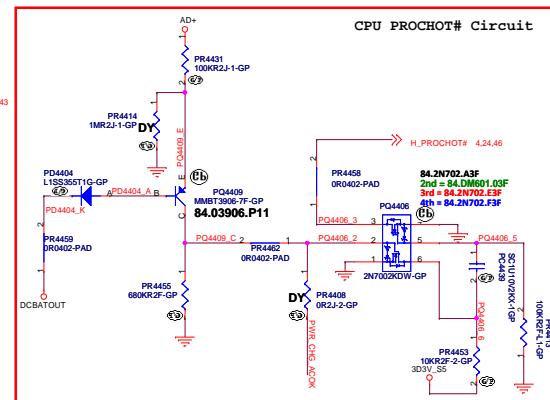
Main Func = Charger



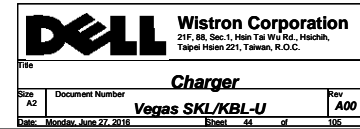
Battery PROCHOT# Circuit



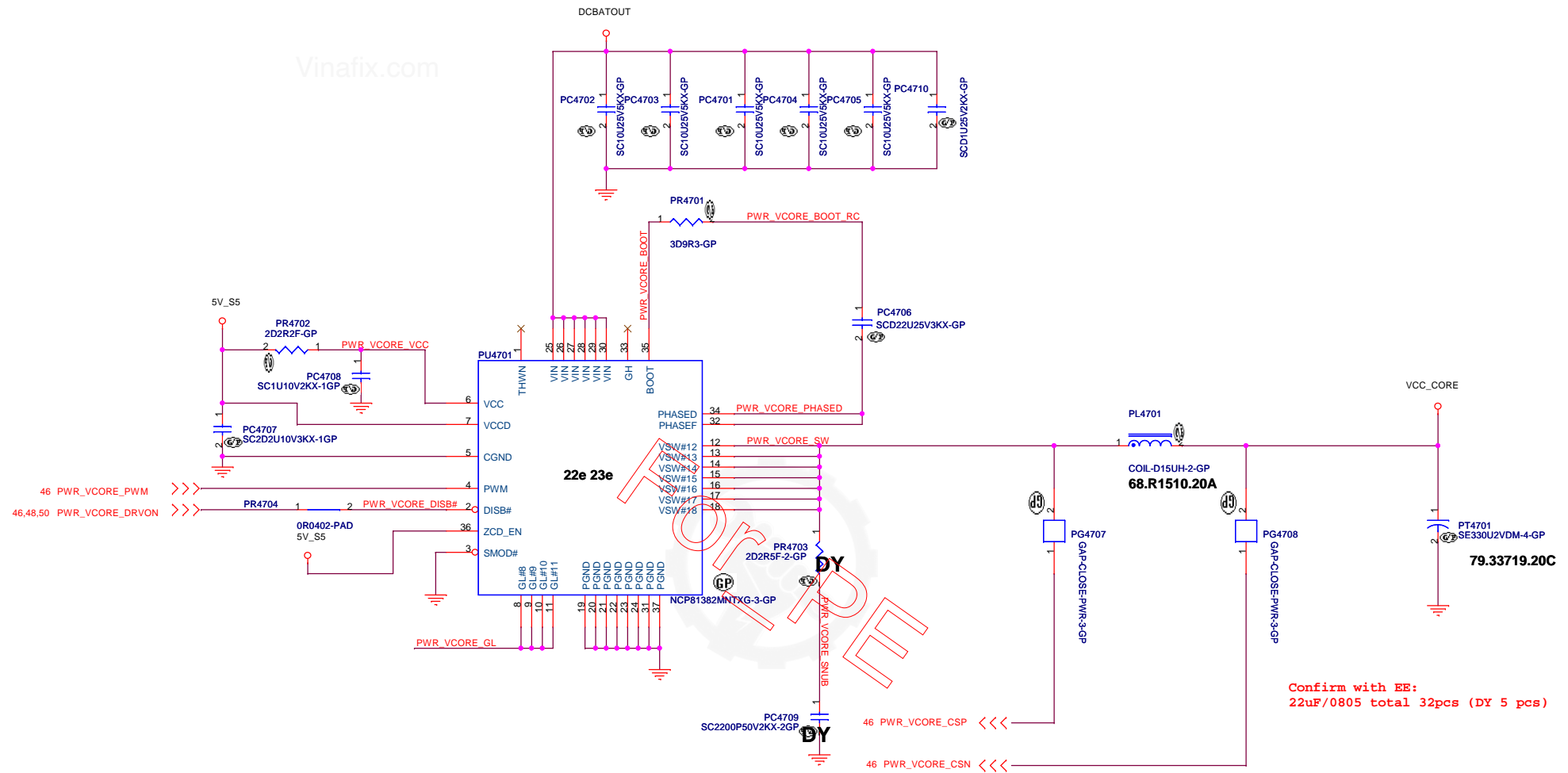
PR4405	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k



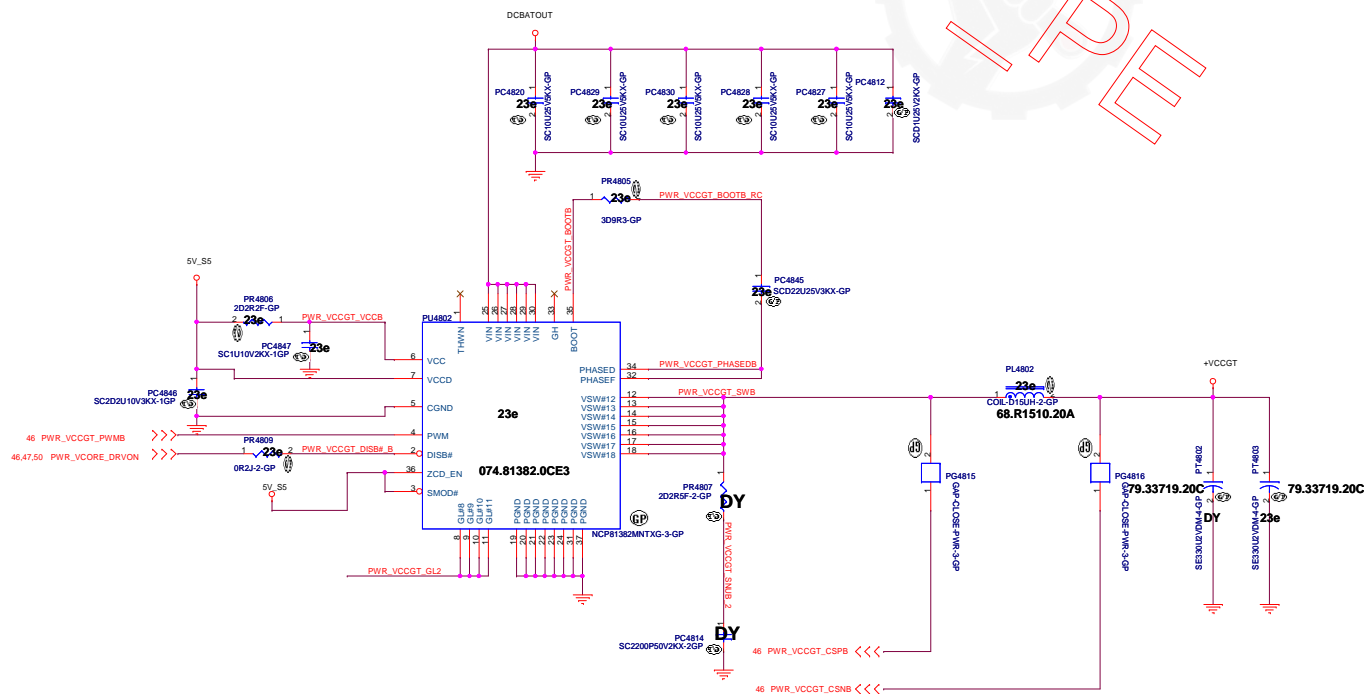
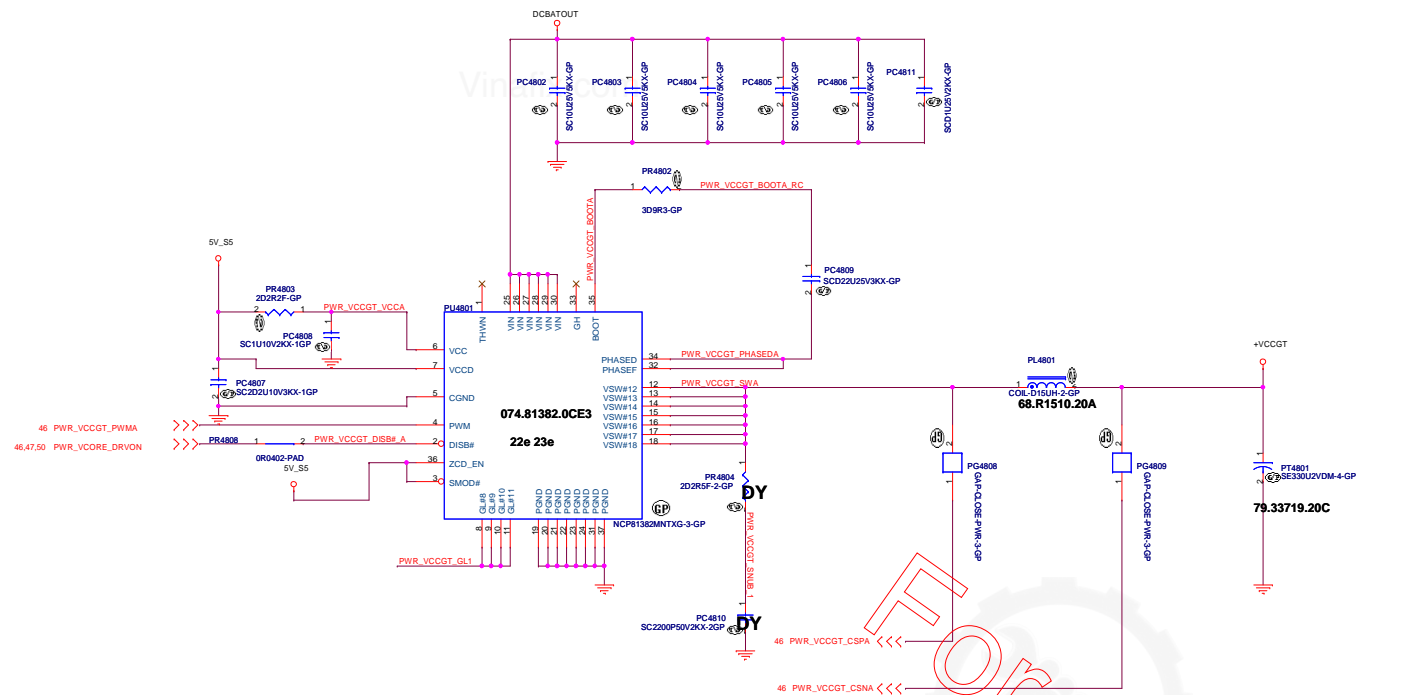
«Core Design



Main Func = CPU_CORE



<Core Design>




<Core Design>

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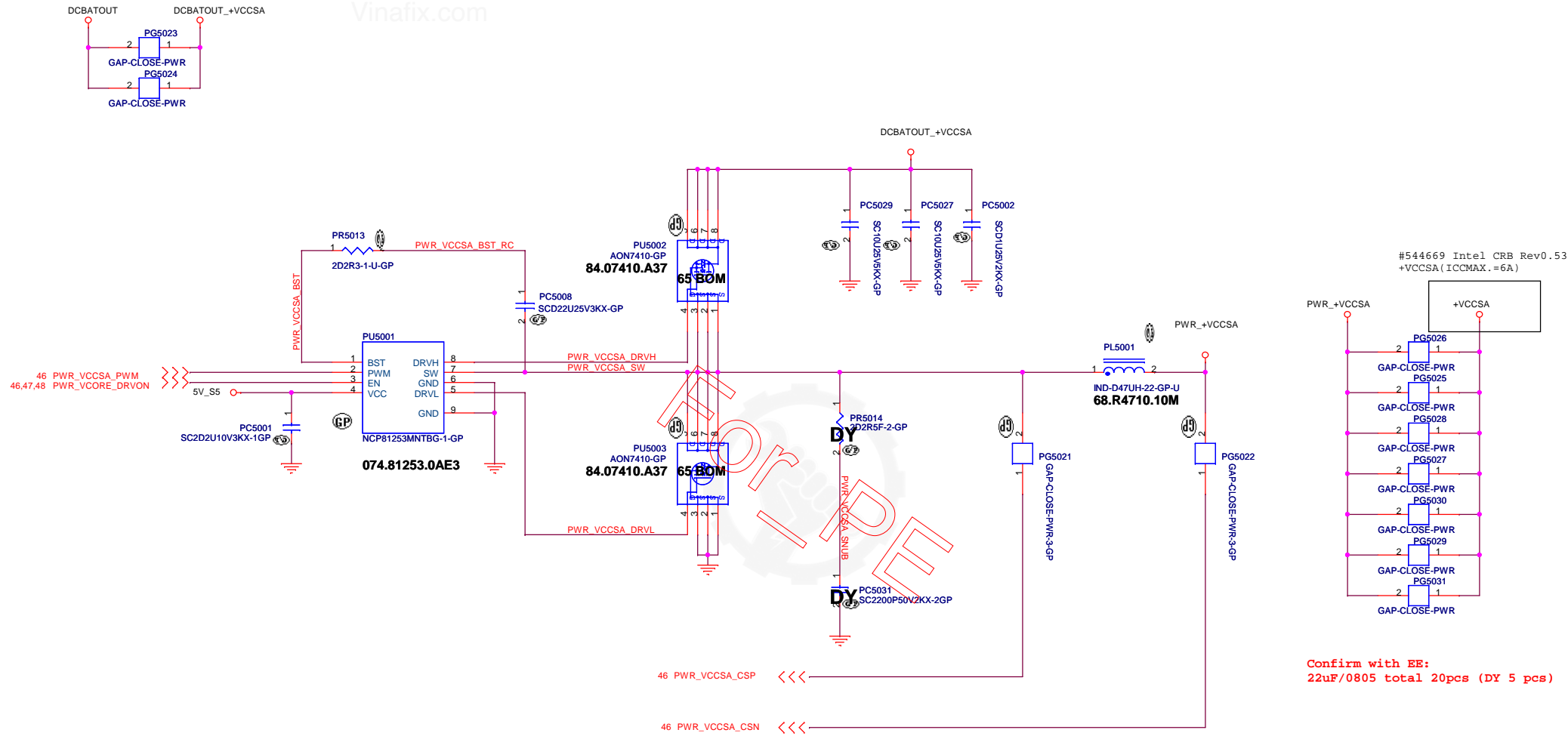


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title NCP81210MN_CPU_VCCGTUS		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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Main Func = CPU_CORE

Vinafix.com



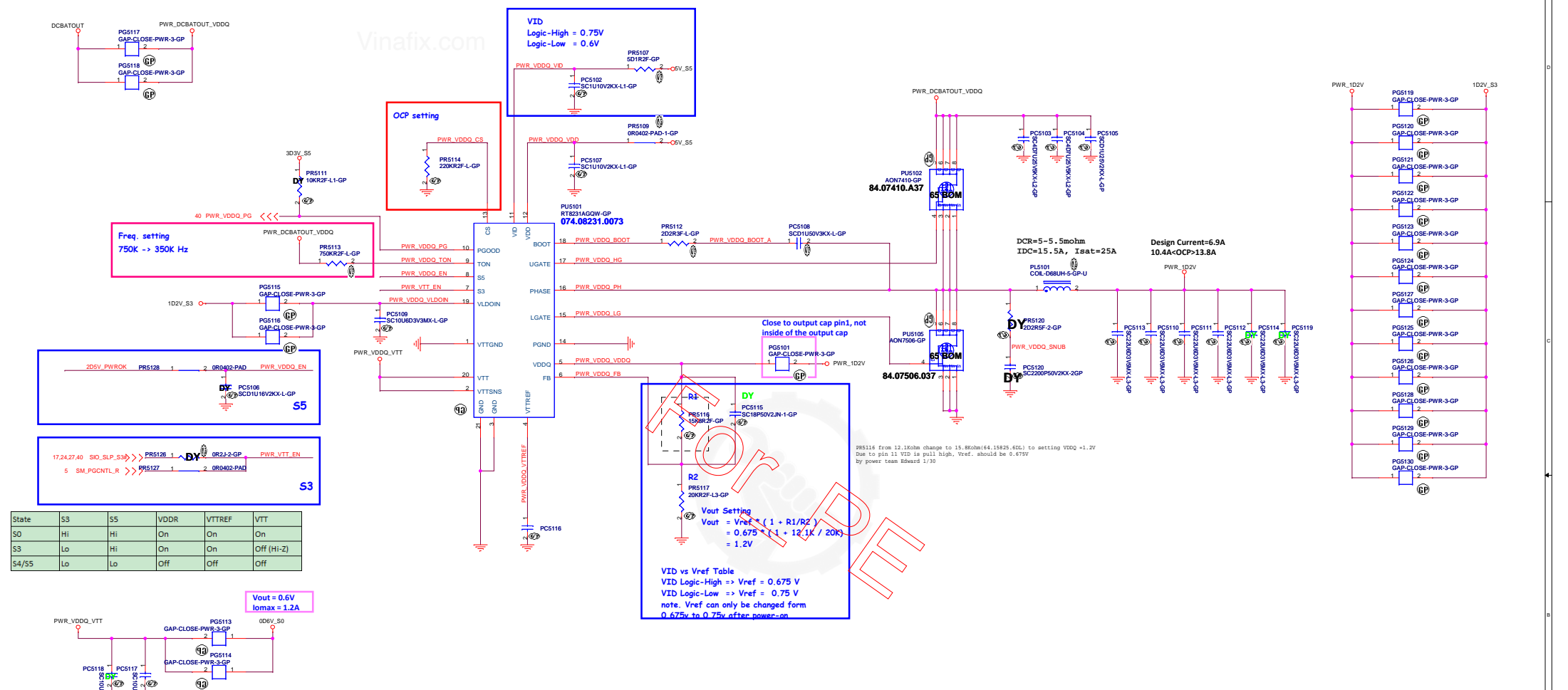
<Core Design>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			NCP81253MN_CPU_VCCSA	
Size	Document Number	Vegas SKL/KBL-U		Rev
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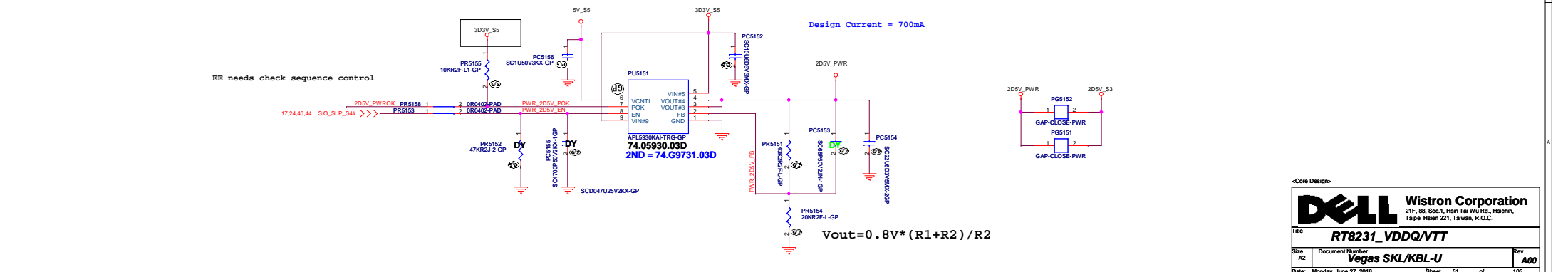
SSID = PWR.Plane.Regulator_1p2v& 2D5V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Vout = 0.6V
Iomax = 1.2A


APL5930 for VPP_2D5V



Vinafix.com

(Blanking)

<Core Design>

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Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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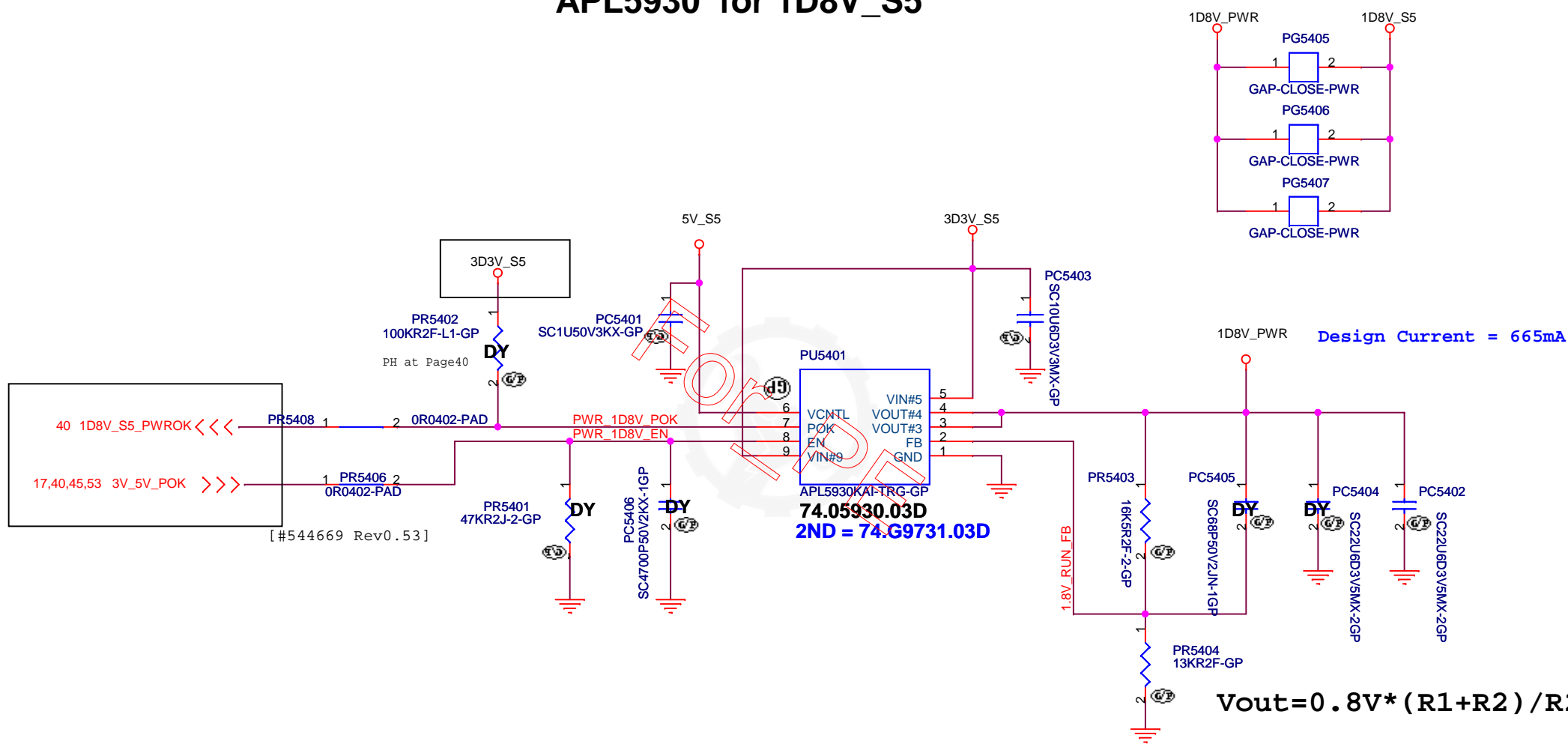
DCR=5~5.5mohm
IDC=15.5A, Isat=25A




Main Func = 1D8V

Vinafix.com

APL5930 for 1D8V_S5



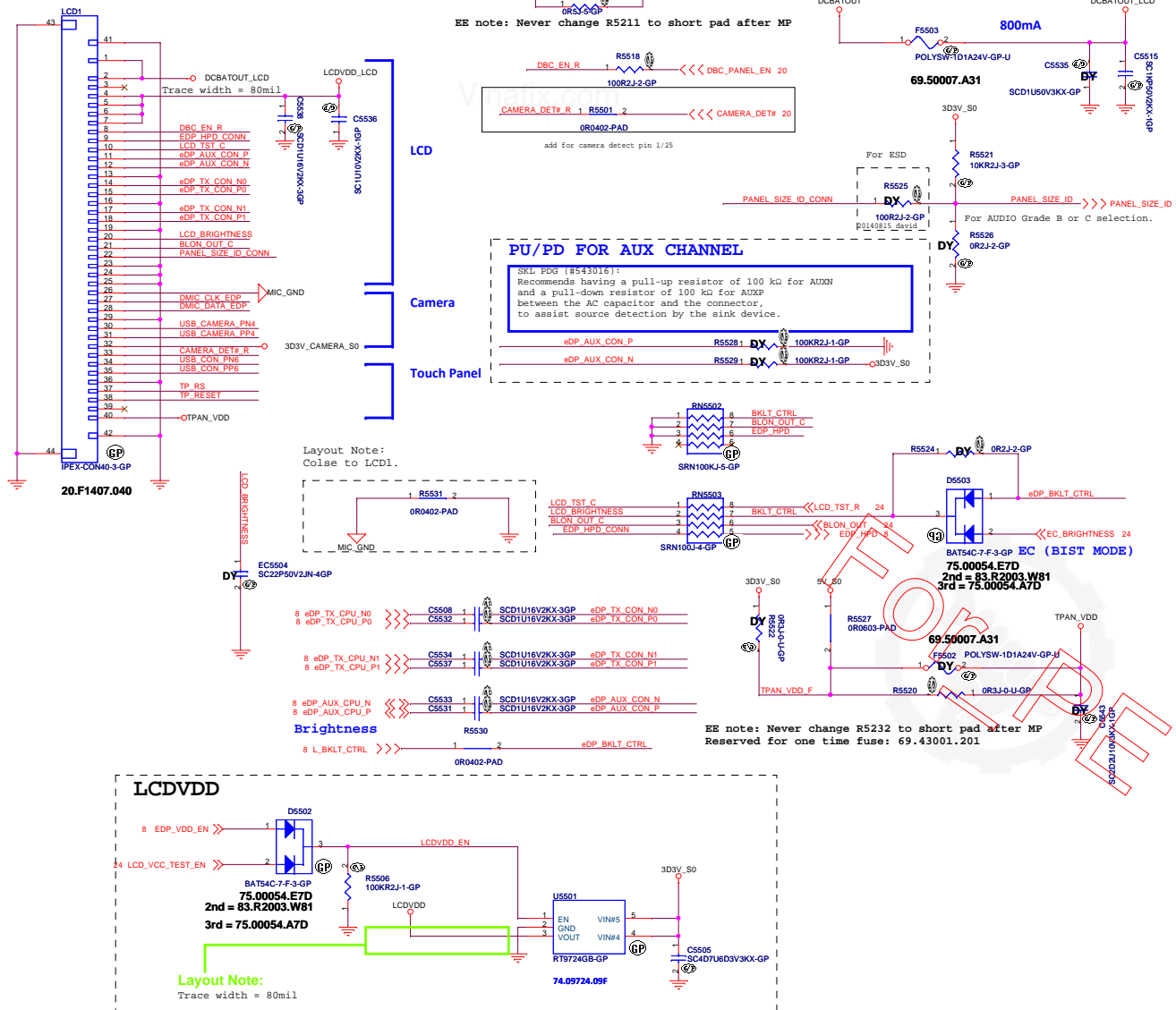
<Core Design>



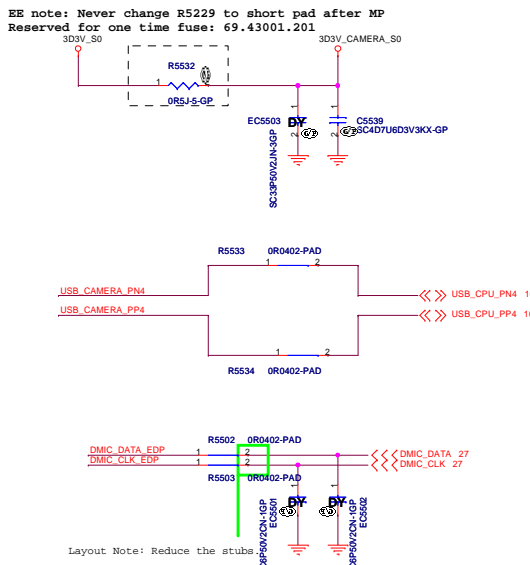
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title LDO-V1D5V&V1D8V		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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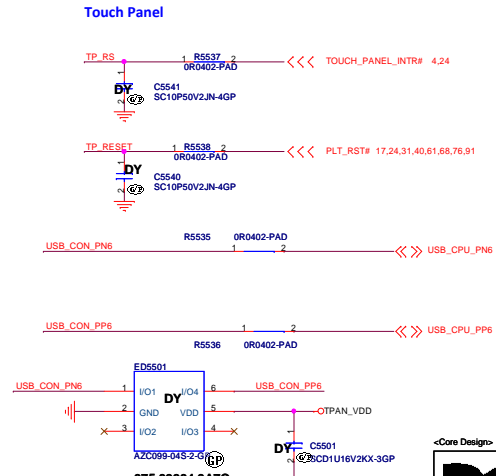
Main Func = LCD



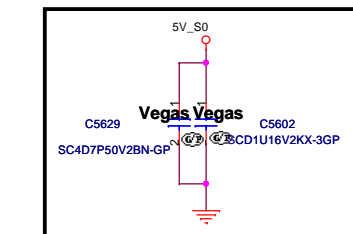
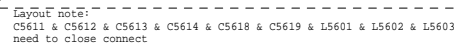
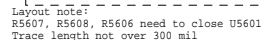
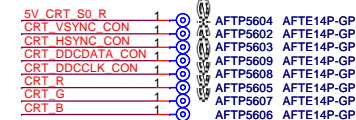
Main Func = CAMERA



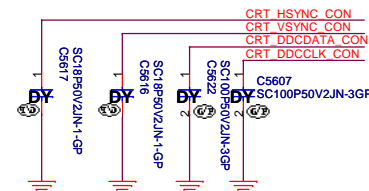
Main Func = Touch panel



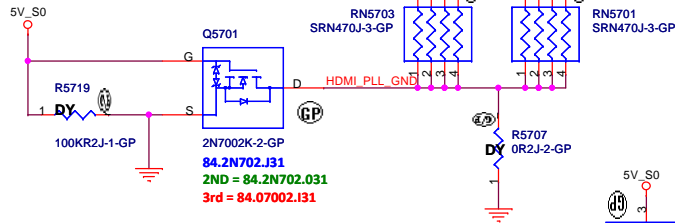
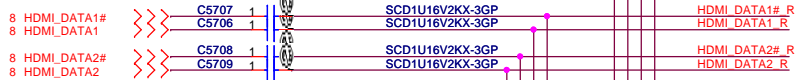
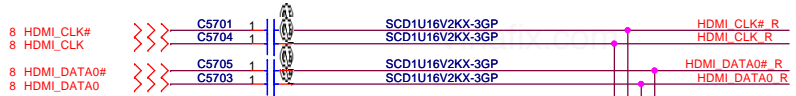
Main Func = CRT



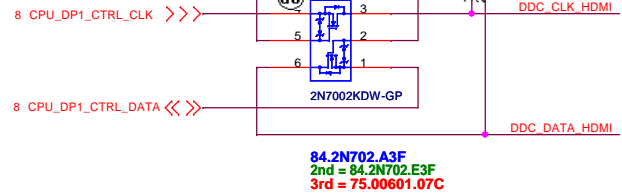
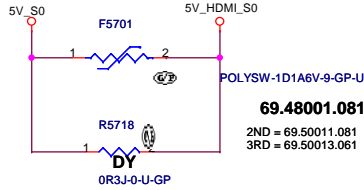
Layout note:
close to pin17



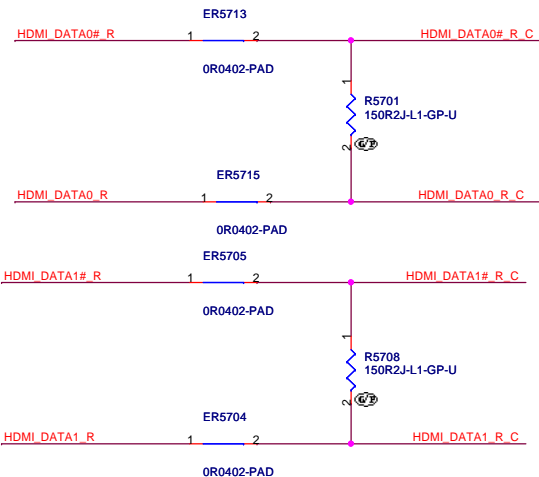
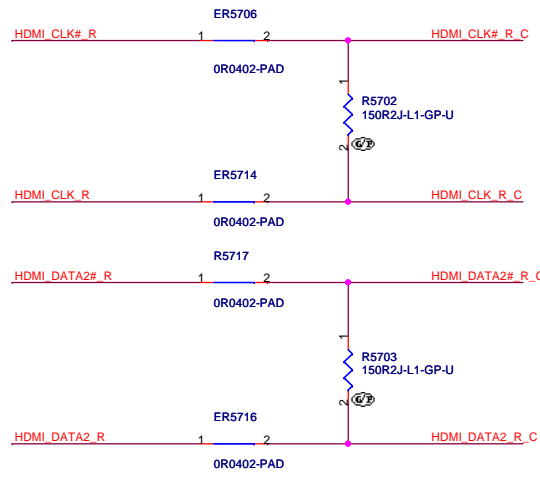
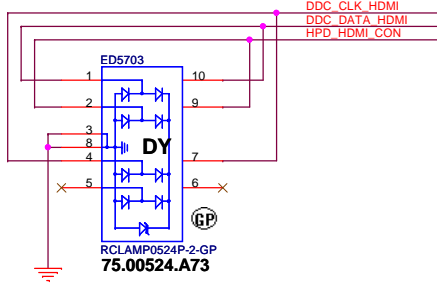
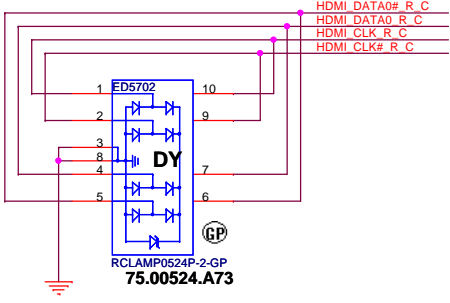
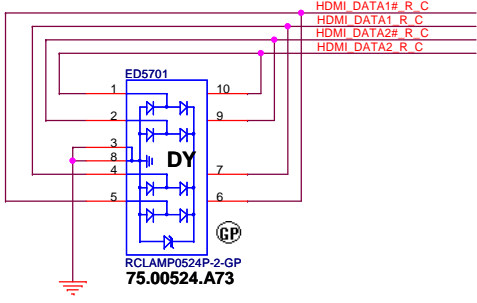
Main Func = HDMI



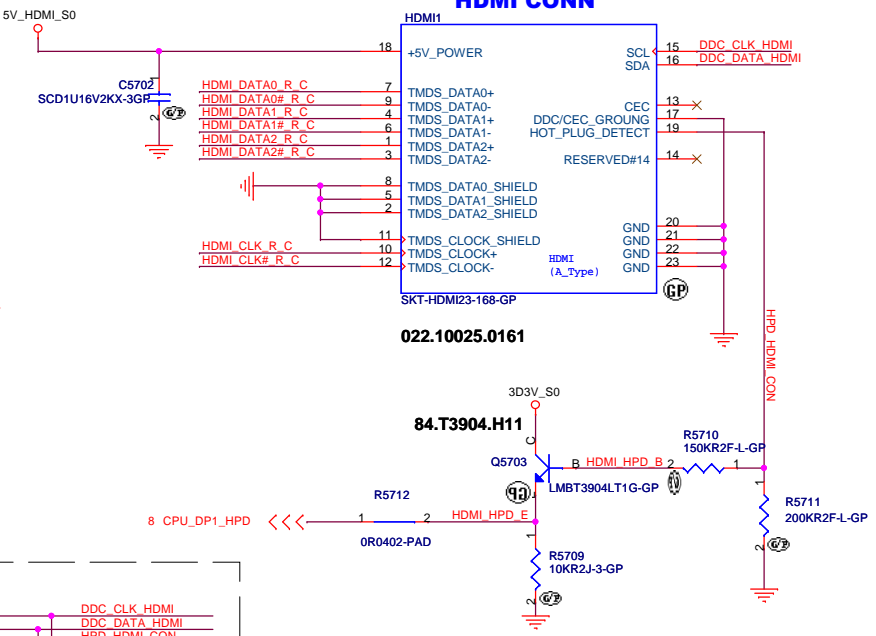
69.50007.691:
OBS REASON: Please transfer to down size item 69.48001.081 for cost reduction and good cost down trend



EMI Request:



HDMI CONN



<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **HDMI**

Size A3	Document Number Vegas SKL/KBL-U	Rev A00
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(Blanking)

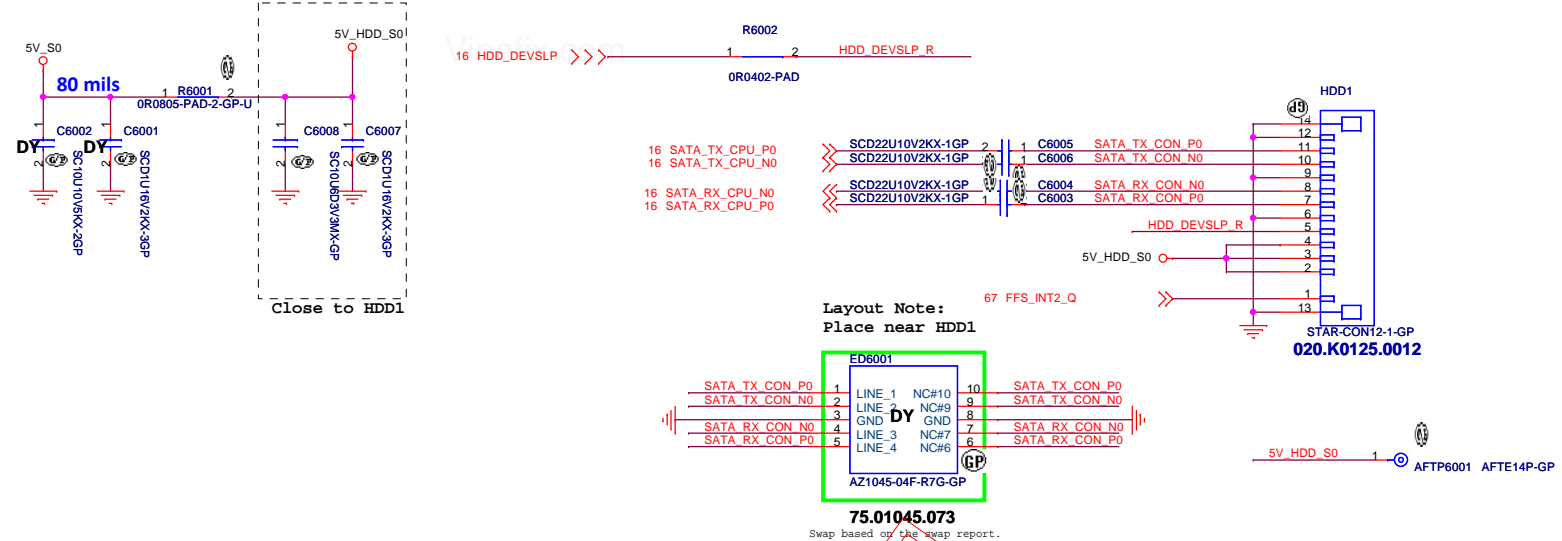


(Blanking)



Main Func = HDD

SATA HDD Connector

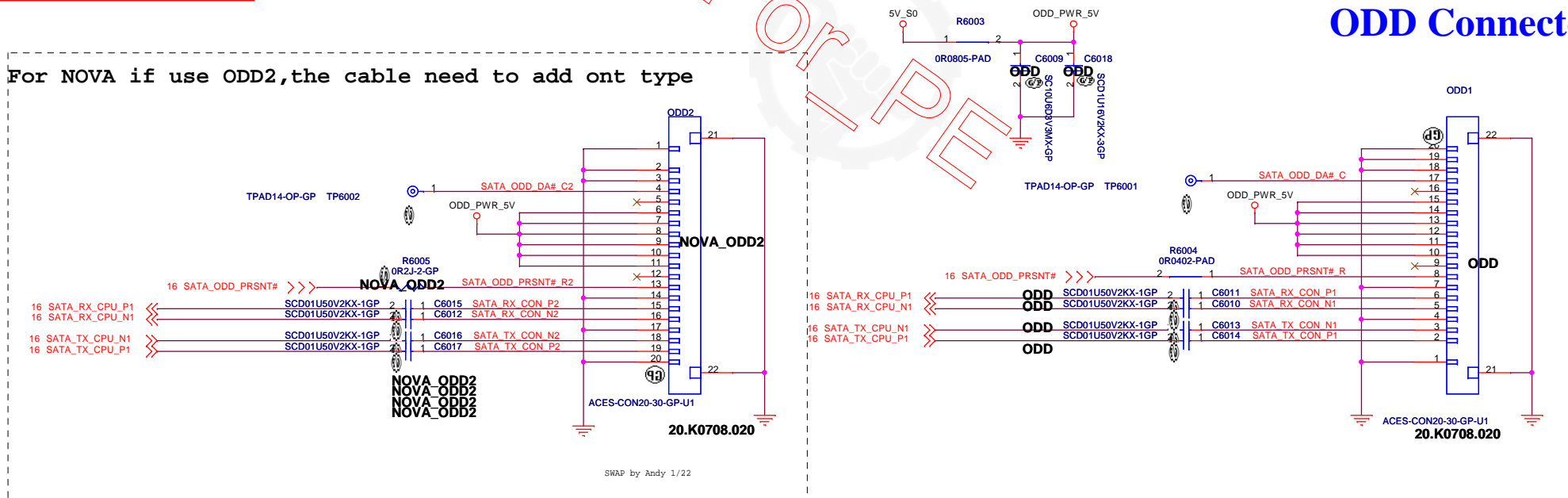


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

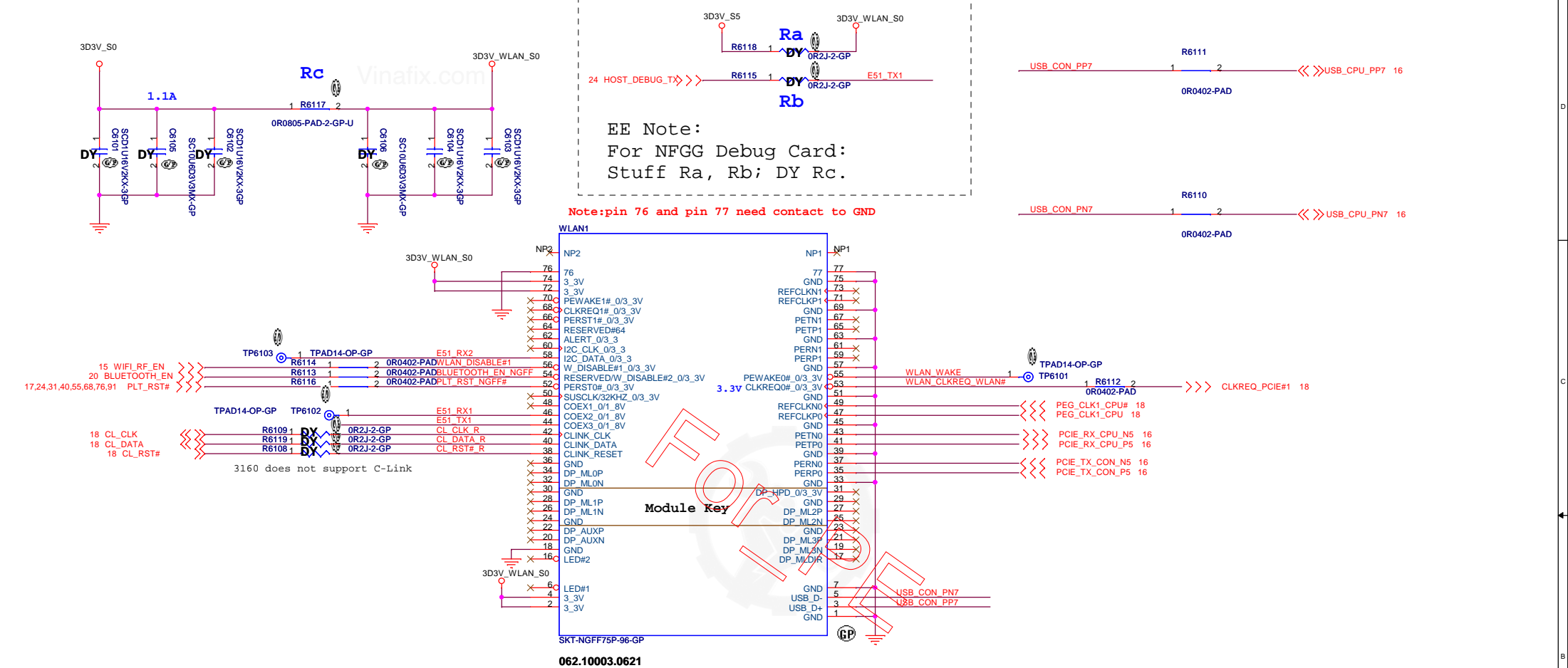
ODD Connector

For NOVA if use ODD2, the cable need to add ont type

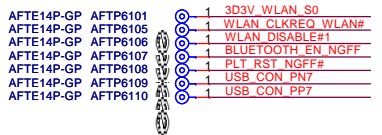


Main Func = WLAN

Reserved for NGFF Debug Card




Support: Intel Dual Band Wireless-AC 3160



(Blanking)




<Core Design>

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Title Reserved			
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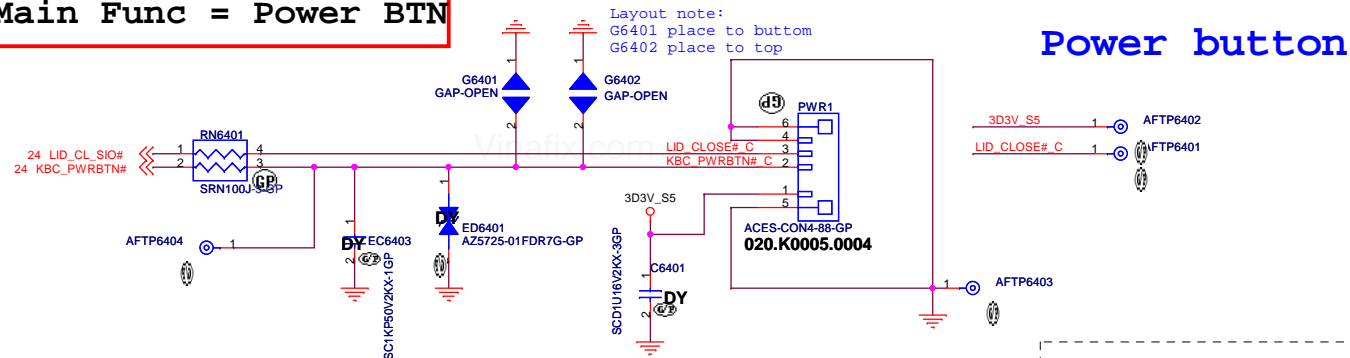
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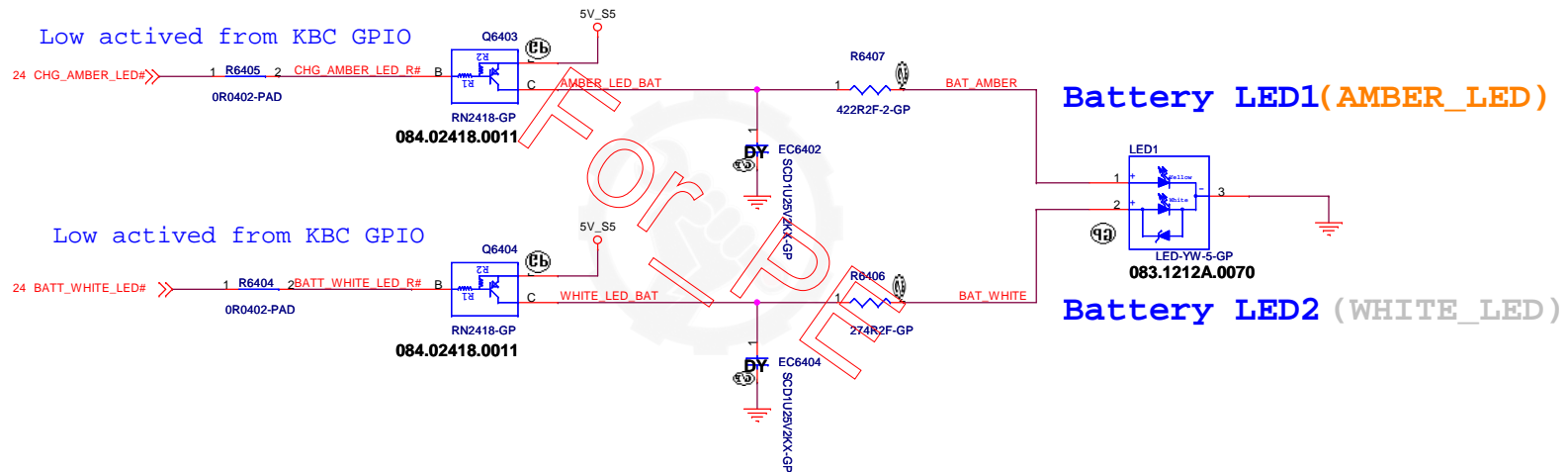
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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Main Func = Power BTN

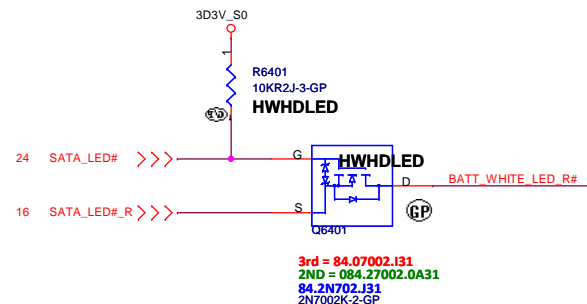


Main Func = Battery LED



Main Func = HDD LED

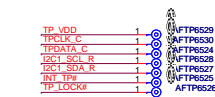
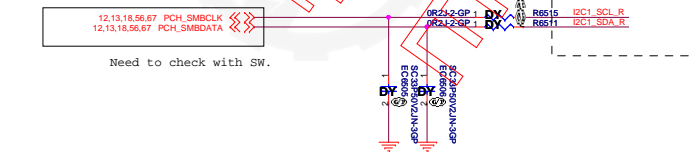
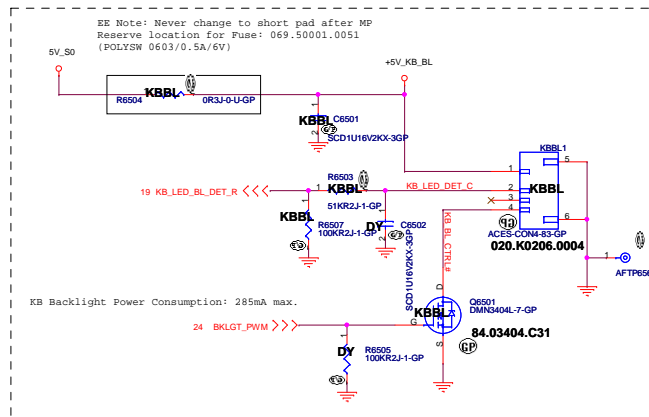
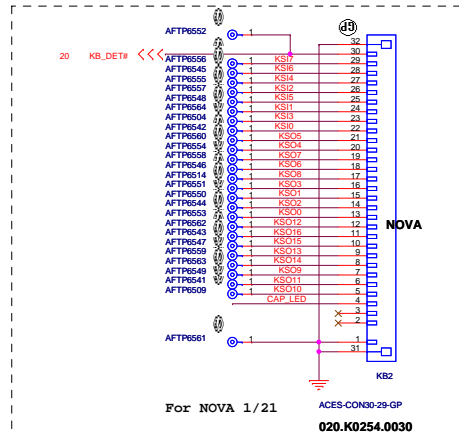
SATA HDD LED
LOW activated from PCH GPIO



<Core Design>

Main Func = TPAD

Precision Touch Pad Connector



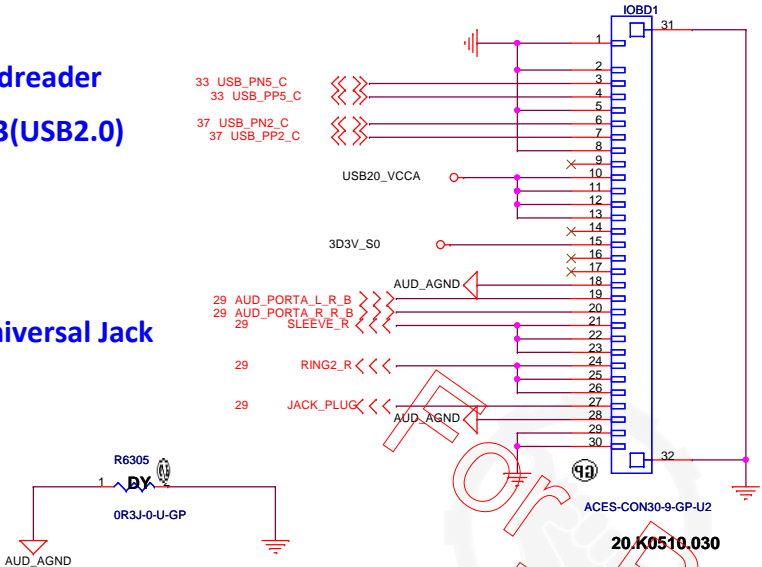
Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(P2)
8	CLK(P2)

Vinafix.com

I/O Board Connector

Cardreader
USB3(USB2.0)

Universal Jack



Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins

USB_PN5_C	1	AFTP6601	AFTE14P-GP
USB_PP5_C	1	AFTP6602	AFTE14P-GP
USB_PN2_C	1	AFTP6603	AFTE14P-GP
USB_PP2_C	1	AFTP6604	AFTE14P-GP
RING2_R	1	AFTP6605	AFTE14P-GP
AUD_PORTA_L_R_B	1	AFTP6606	AFTE14P-GP
JACK_PLUG	1	AFTP6607	AFTE14P-GP
AUD_PORTA_R_R_B	1	AFTP6608	AFTE14P-GP
SLEEVE_R	1	AFTP6609	AFTE14P-GP
USB20_VCCA	1	AFTP6610	AFTE14P-GP
AUD_AGND	1	AFTP6611	AFTE14P-GP
	1	AFTP6612	AFTE14P-GP

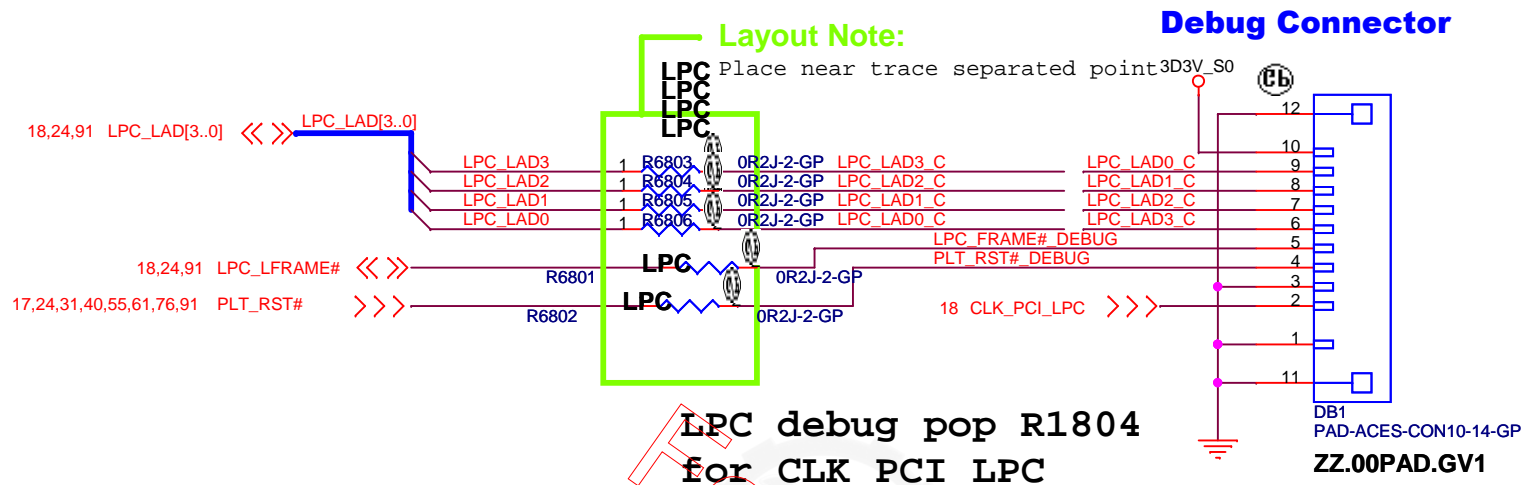
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Title			
IO Board Connector			
Size	Document Number	Rev	
A3	Vegas SKL/KBL-U	A00	
Date:	Monday, June 27, 2016	Sheet	66 of 105

Main Func = Debug

Vinafix.com



LPC debug pop R1804
for CLK_PCI_LPC

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>



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Title

Dubug connector

Size
A4

Document Number

Vegas SKL/KBL-U

Rev
A00

Date: Monday, June 27, 2016

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Title

Reserved

Size
A4

Document Number

Vegas SKL/KBL-U

Rev
A00

Date: Thursday, June 16, 2016

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Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
Date: Thursday, June 16, 2016		Sheet 70 of	105

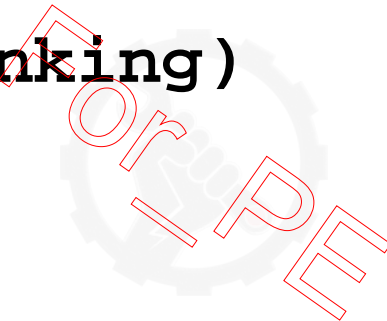
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Title			
RESERVED			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
Date:	Thursday, June 16, 2016		Sheet 71 of 105

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Title USB3.0 PORT		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Thursday, June 16, 2016		Sheet 72 of 105

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For PE

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Title

Reserved

Size
A4

Document Number

Vegas SKL/KBL-U

Rev
A00

Date: Thursday, June 16, 2016

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Main Func = dGPU

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GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω
GPU1A

1 OF 7

16 PEG_TX_GPU_P0
16 PEG_TX_GPU_N0

16 PEG_TX_GPU_P1
16 PEG_TX_GPU_N1

16 PEG_TX_GPU_P2
16 PEG_TX_GPU_N2

16 PEG_TX_GPU_P3
16 PEG_TX_GPU_N3

>>>
>>>
>>>
>>>

AF30
AC31

AE29
AD28

AD30
AC31

AC29
AB28

PCIE_RX0P
PCIE_TX0N

PCIE_RX1P
PCIE_RX1N

PCIE_RX2P
PCIE_RX2N

PCIE_RX3P
PCIE_RX3N

AB30
AA31

AA29
Y28

Y30
W31

W29
V28

PCIE_RX4P
PCIE_RX4N

PCIE_RX5P
PCIE_RX5N

PCIE_RX6P
PCIE_RX6N

PCIE_RX7P
PCIE_RX7N

Y30
U31

U29
T28

T30
R31

P29
P28

P30
N31

NC#V30
NC#U31

NC#U29
NC#T28

NC#T30
NC#R31

NC#R29
NC#P28

NC#P30
NC#N31

N29
M28

M30
L31

L29
K30

NC#N29
NC#M28

NC#M30
NC#L31

NC#L29
NC#K30

FOR REFERENCE

PCI EXPRESS INTERFACE

PCIE_TX0P
PCIE_TX0N

PCIE_TX1P
PCIE_TX1N

PCIE_TX2P
PCIE_TX2N

PCIE_TX3P
PCIE_TX3N

PCIE_TX4P
PCIE_TX4N

PCIE_TX5P
PCIE_TX5N

PCIE_TX6P
PCIE_TX6N

PCIE_TX7P
PCIE_TX7N

NC#W24
NC#W23

NC#V27
NC#U26

NC#U24
NC#U23

NC#T26
NC#T27

NC#T24
NC#T23

NC#P27
NC#P26

NC#P24
NC#P23

NC#M27
NC#N26

NC#M27
NC#N26

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

Table 3-5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

DGPU_HOLD_RST#

H	dGPU mode
L	IGPU
H	IGPU with BACO

20 DGPU_HOLD_RST#

17,24,31,40,55,61,68,91 PLT_RST#

3D3V_VGA_S0

R7625

10KR2J-3-GP

DY

R7623

0R0402-PAD

D7601

BAW56-5-GP

DY

ATI_RST#

R7621

0R0402-PAD

VGA_RST#

AL27

PERST#

JET-XT-S3-GP

OPS

C7609

SC47P50V2JN-3GP

DY

3D3V_VGA_S0

R7601

1KR2F-3-GP

OPS

PWRGOOD_TEST

N10

TEST_PG

PERST#

JET-XT-S3-GP

18 PEG_CLK_CPU

18 PEG_CLK_CPU#

AK30

AK32

PCIE_REFCLKP

PCIE_REFCLKN

TEST_PG

PERST#

JET-XT-S3-GP

OPS

C7609

SC47P50V2JN-3GP

DY

3D3V_VGA_S0

R7601

1KR2F-3-GP

OPS

PWRGOOD_TEST

N10

TEST_PG

PERST#

JET-XT-S3-GP

OPS

C7609

SC47P50V2JN-3GP

DY

3D3V_VGA_S0

R7601

1KR2F-3-GP

CALIBRATION

PCIE_CALR_TX

PCIE_CALR_RX

Y22

AA22

PCIE_CALR_TX

PCIE_CALR_RX

1K69R2F-2-GP

OPS

1

R7622

OD95V_VGA_S0

OPS

1

R7618

PCIE_CALR_TX

PCIE_CALR_RX

1K69R2F-2-GP

OPS

1

R7618

PCIE_CALR_TX

PCIE_CALR_RX

1K69R2F-2-GP

OPS

1

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Title

076_GPU(1/5) PEG

Size

Project Name

Rev

Date

Monday, June 27, 2016

<Project Name>

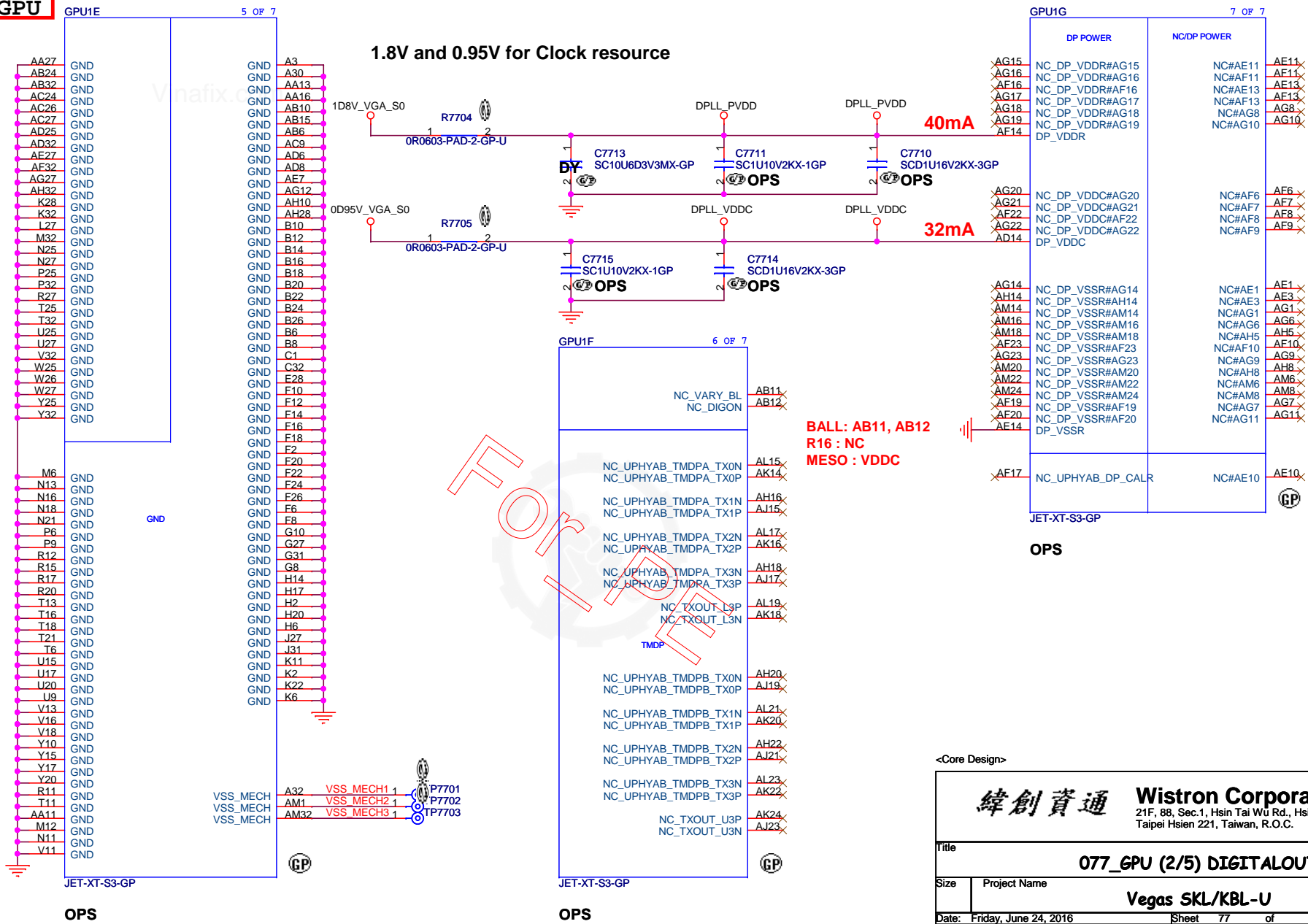
Sheet

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of

105

Main Func = dGPU



<Core Design>

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Title	077_GPU (2/5) DIGITALOUT
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Size	Project Name	Rev
	Vegas SKL/KBL-U	X00
Date: Friday, June 24, 2016	Sheet 77 of 105	

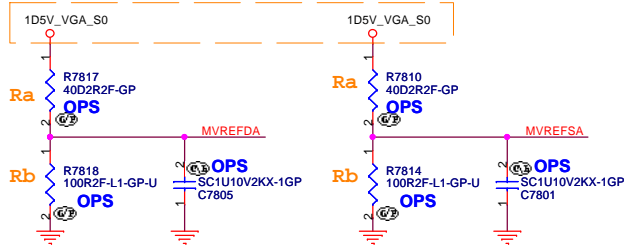
Main Func = dGPU

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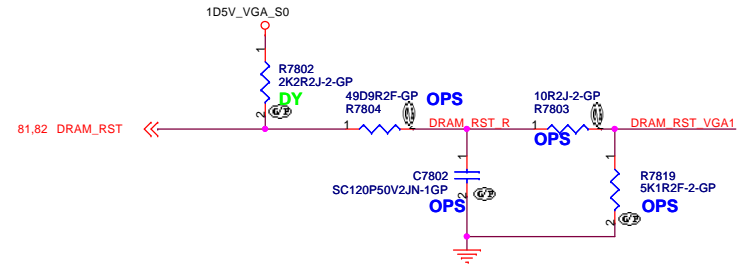
Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

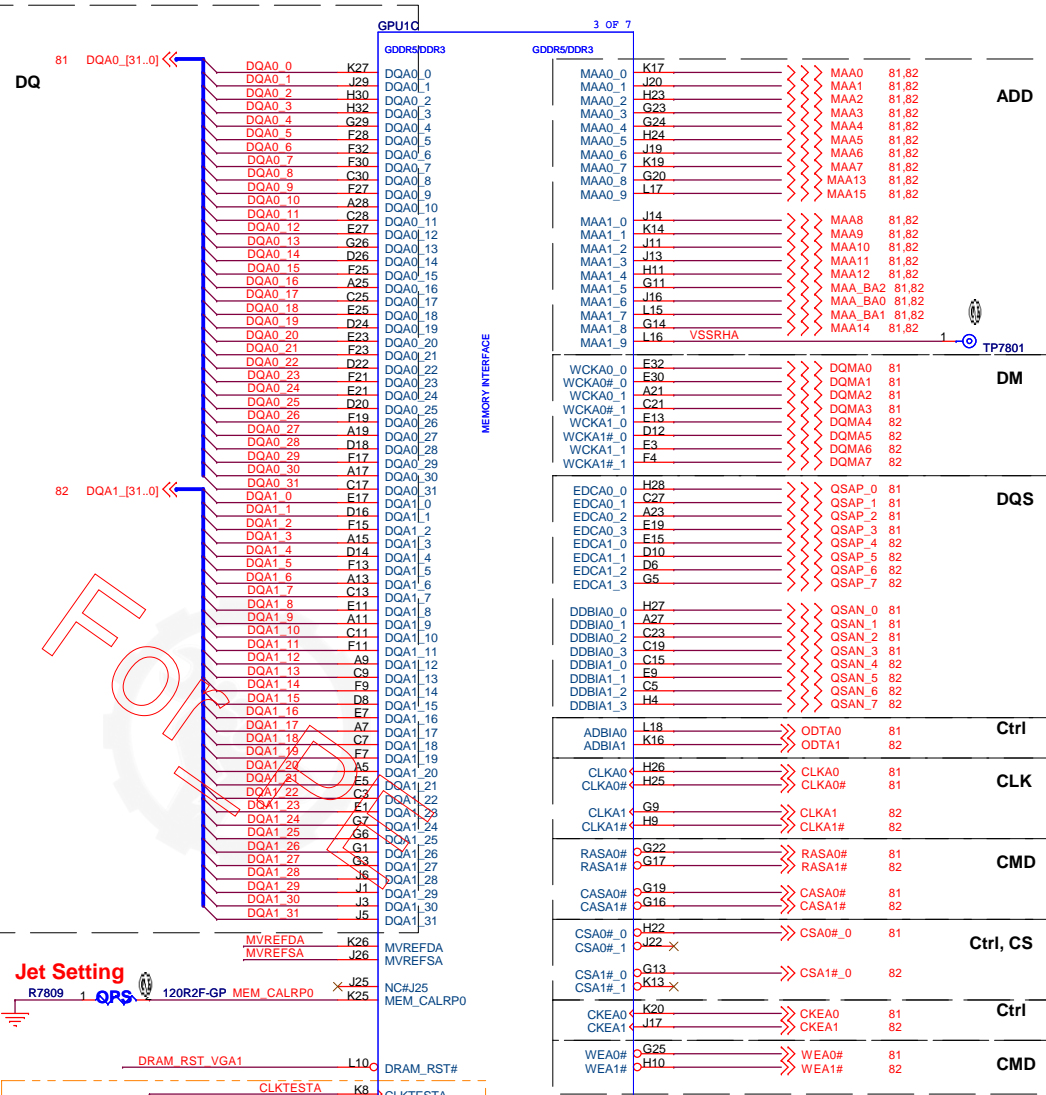
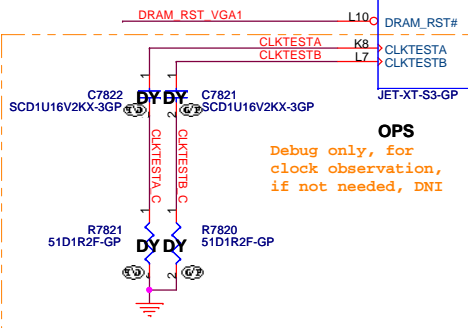
	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Place all these componets very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR3



Jet Setting
R7809 120R2F-GP MEM_CALRP0



<Core Design>

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Title	078_GPU (3/5) VRAM I/F	Rev
Size	Project Name	
Vegas SKL/KBL-U		
Date: Monday, June 27, 2016	Sheet 78	of 105

3

2

Title		07
Size	Project Name	
Date	Monday, June 27, 2016	

PU (4/5) GPIO/STRAP	
Regas SKL/KBL-U	Rev
Sheet 79 of 105	

Age Group	Percentage
18-24	15%
25-34	25%
35-44	20%
45-54	15%
55-64	10%
65-74	5%
75-84	5%
85+	5%

2

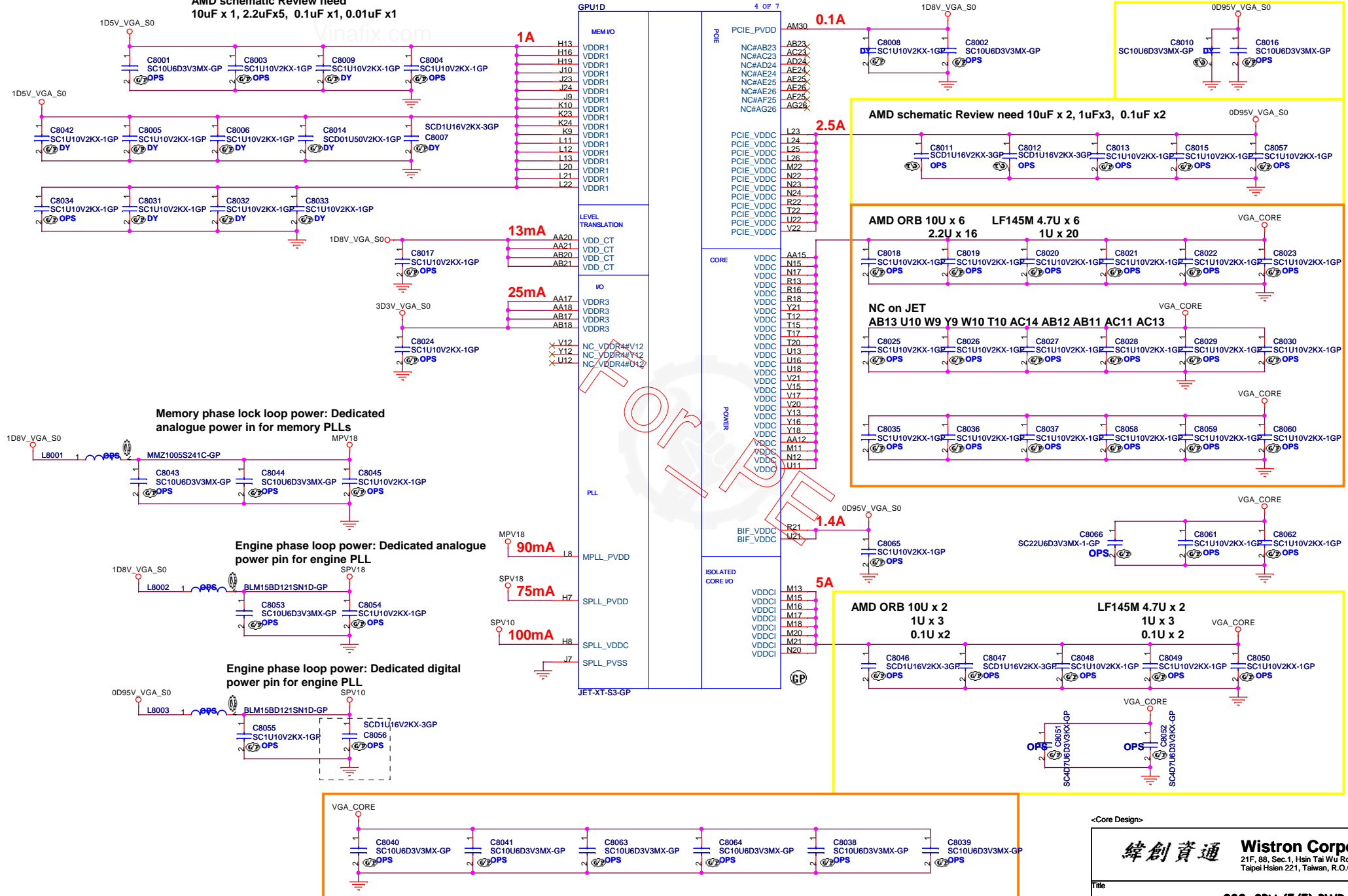
Page	Project Name
Date	Monday, June 27, 2016

egas SKL/KBL-U

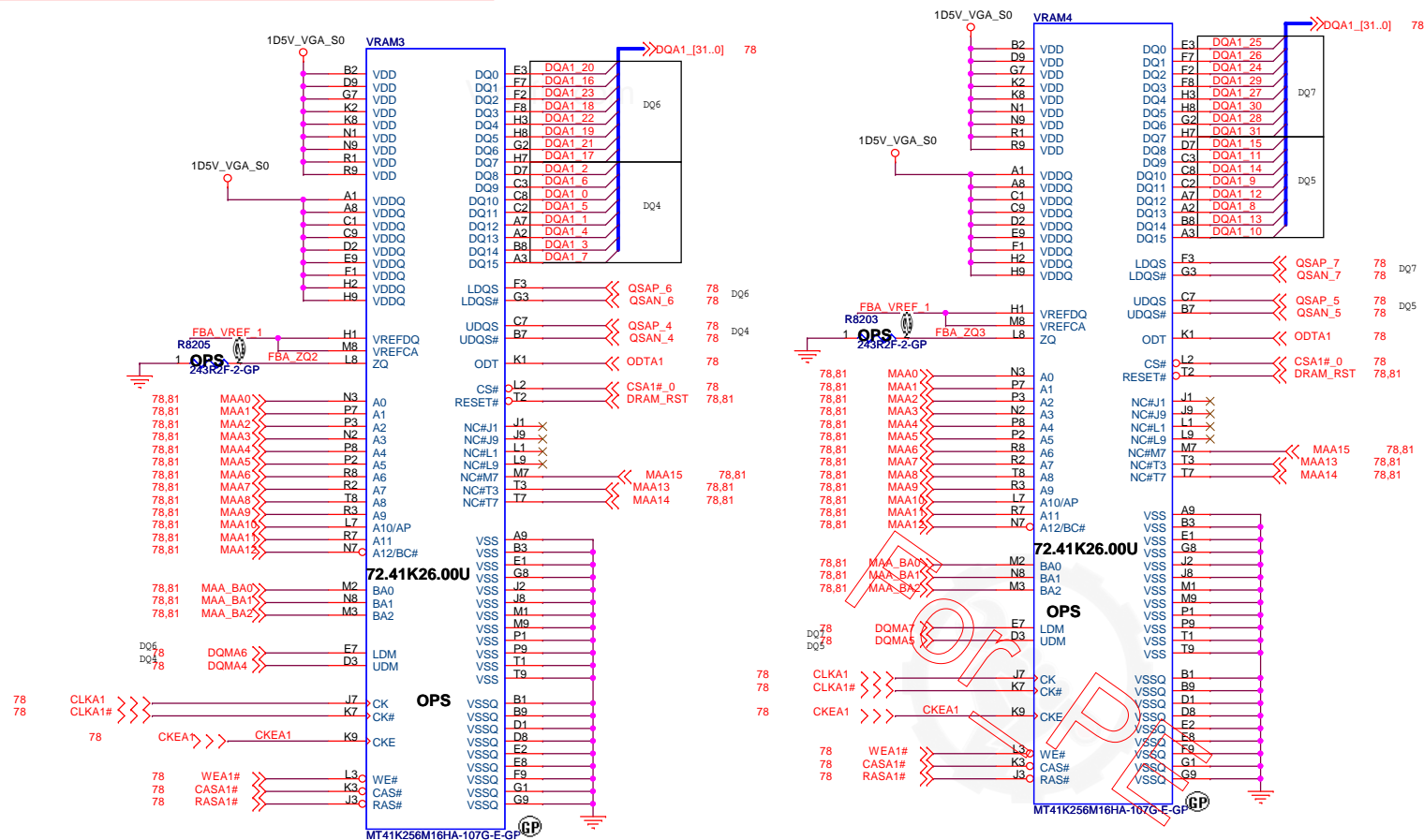
Sheet 79 of 105


```
Main Func = dGPU
```

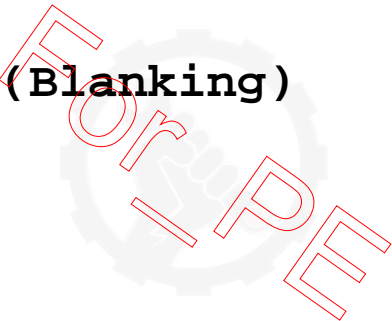
AMD schematic Review need
10uF x 1, 2.2uFx5, 0.1uF x1, 0.01uF x1



Main Func = Vram (DDR3L)



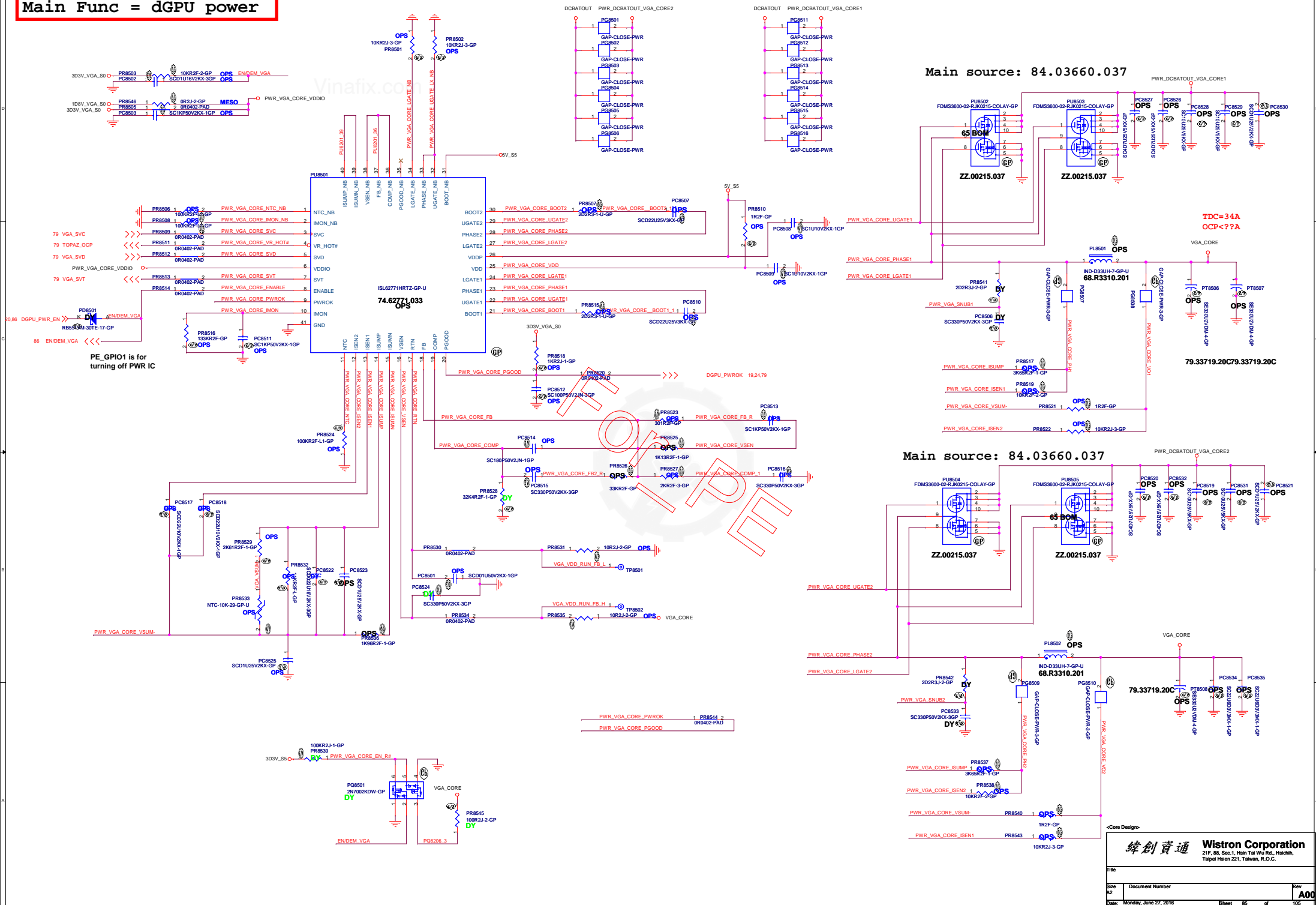
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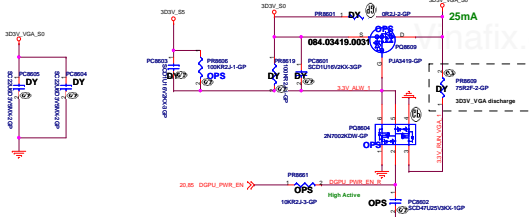


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Main Func = dGPU power



3D3V_S0 to 3D3V_VGA_S0 Transfer



GPU PWR Sequencing

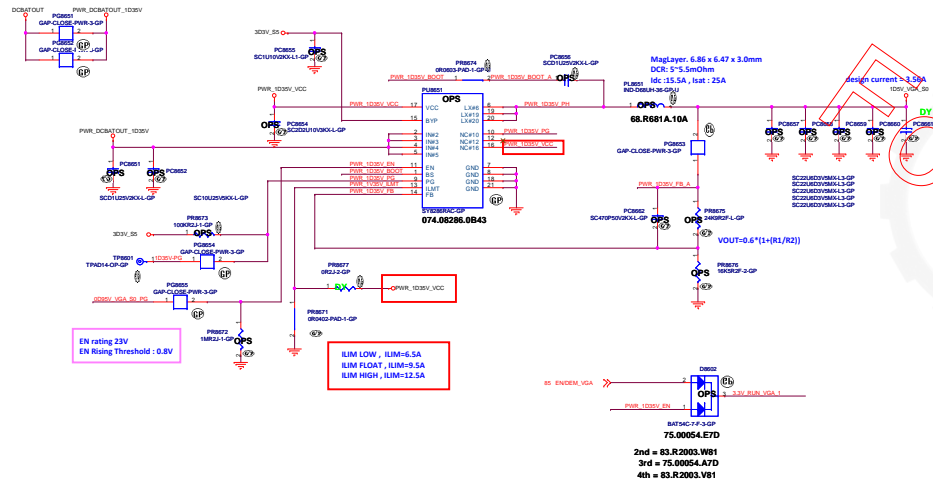
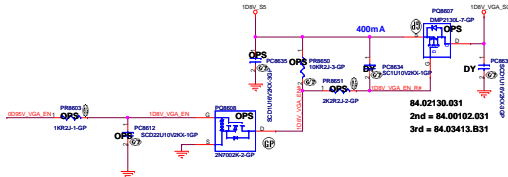
3D3V_VGA_S0

- => 0D95V_VGA_S0/1D8V_VGA_S0
- => 1D5V_VGA_S0
- => VGA_CORE

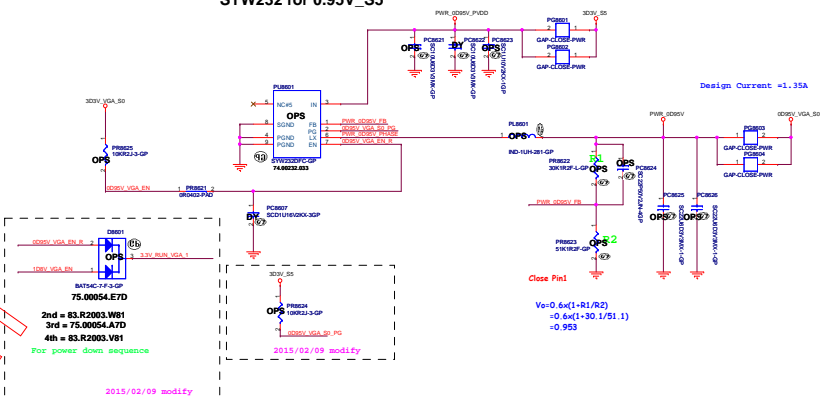
All the ASIC supplies must reach their respective nominal voltages within **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



SYW232 for 0.95V_S5



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Title

Reserved

Size
A4

Document Number

Vegas SKL/KBL-U

Rev

A00


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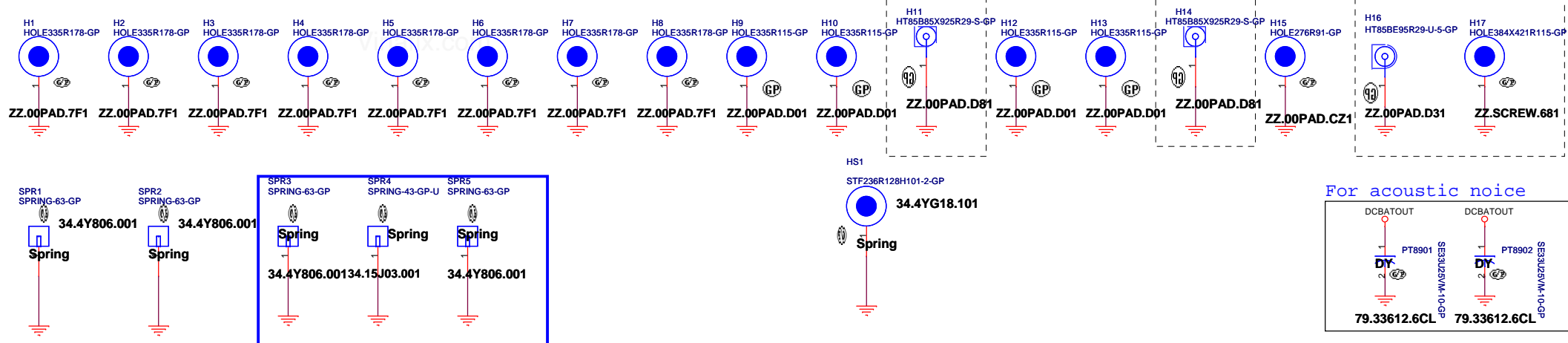
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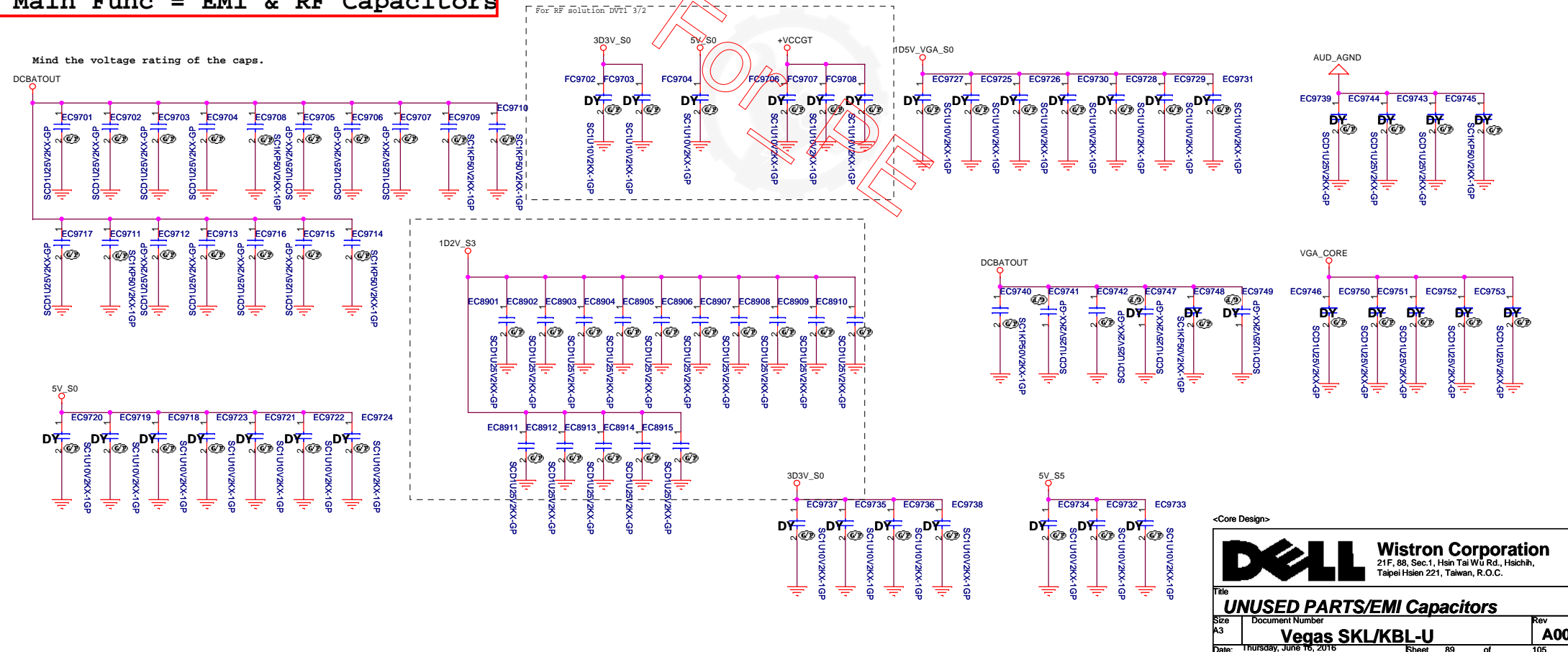
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Title Reserved			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = UnusedParts




Main Func = EMI & RF Capacitors



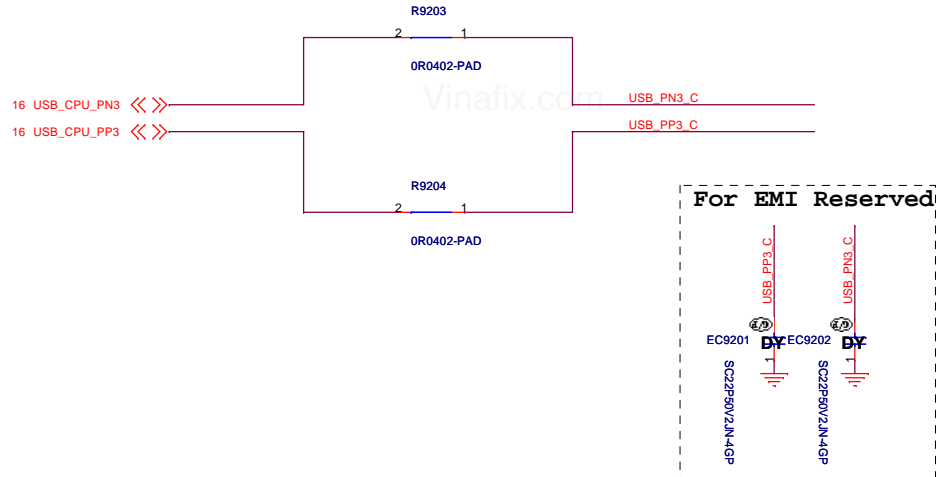
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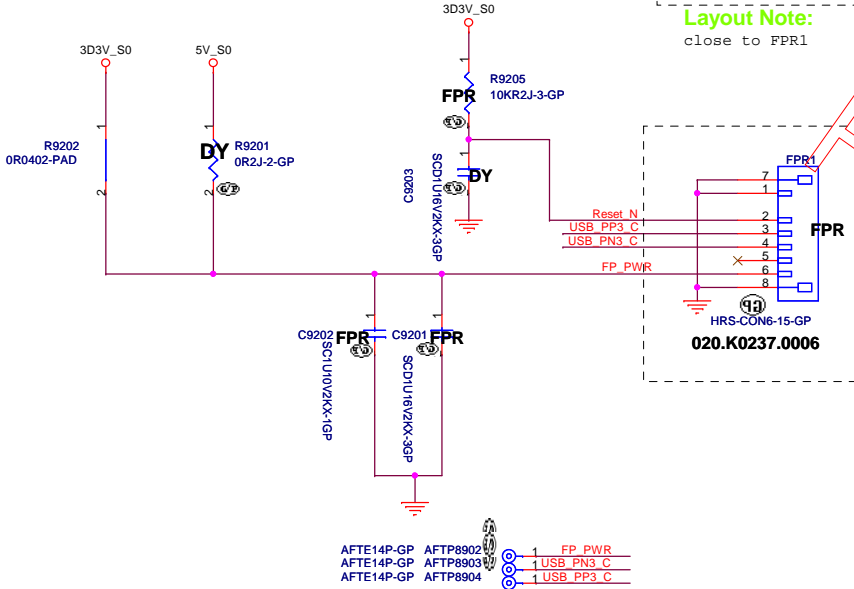
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Title Reserved		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Thursday, June 16, 2016		Sheet 90 of 105

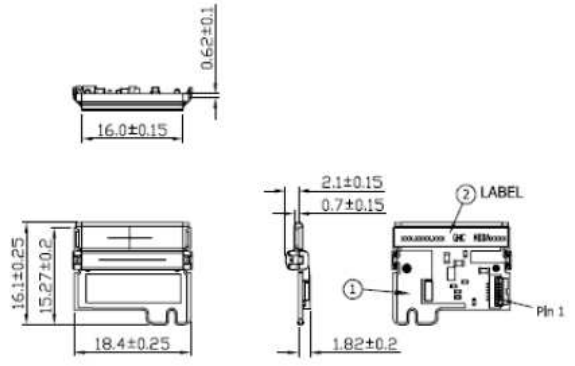
SSID = Finger Print



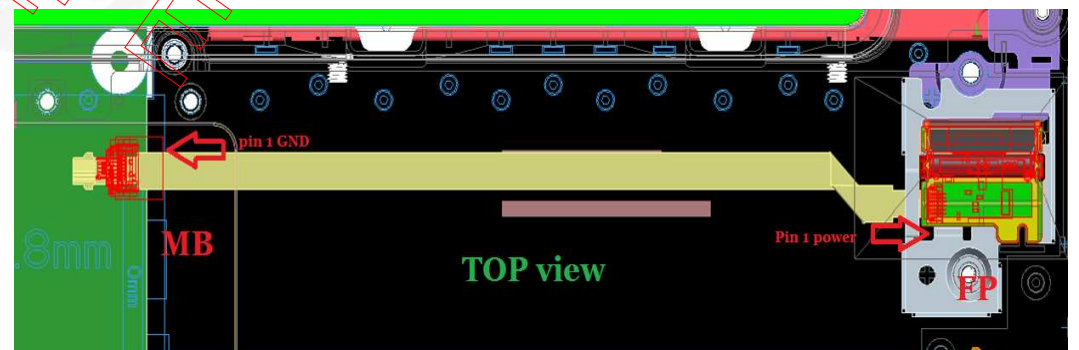
Layout Note:
close to FPR1



- AFTE14P-GP AFTP8902 1 FP_PWR
- AFTE14P-GP AFTP8903 1 USB_PN3_C
- AFTE14P-GP AFTP8904 1 USB_PP3_C



Note :
Module:
1.Sensor Type;Semiconductor
2.Interface:USB 1.0 and 2.0 Full Speed




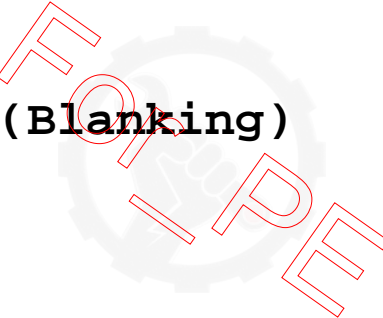
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Title			
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Size A3	Document Number Vegas SKL/KBL-U		Rev A00
Date: Thursday, June 16, 2016		Sheet 93	of 105




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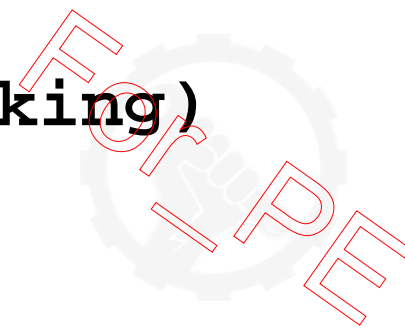
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Size A3	Document Number Vegas SKL/KBL-U		Rev A00
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Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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<Core Design>



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Title

LVDS_Switch

Size
A4

Document Number

Vegas SKL/KBL-U

Rev
A00

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A

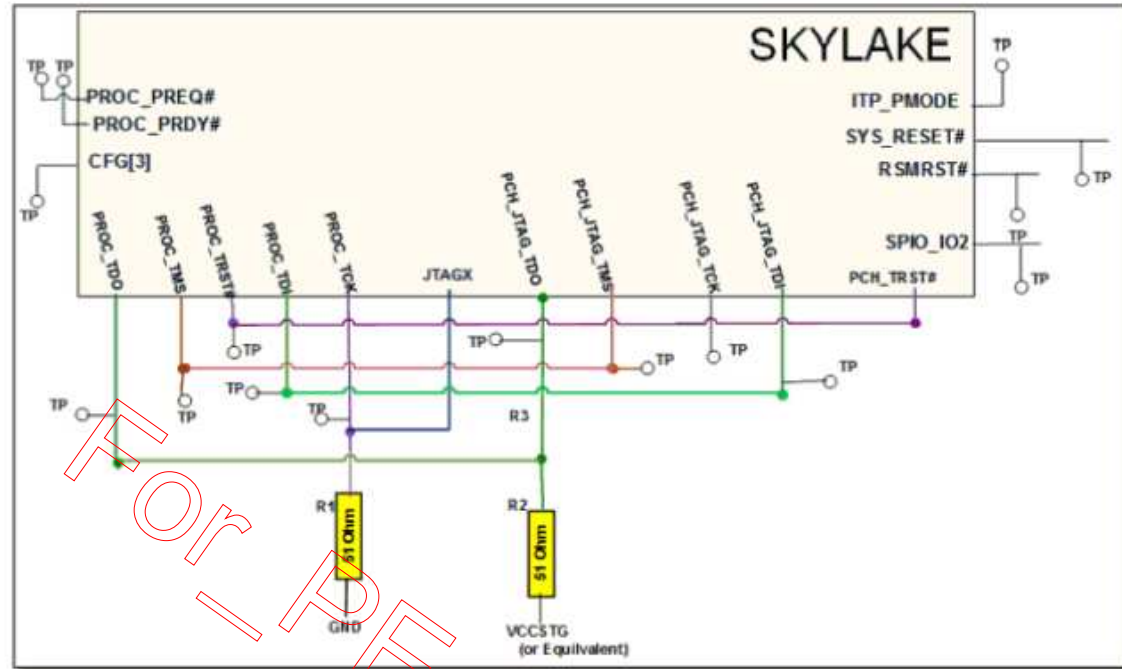
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Title			
CRT Switch			
Size A3	Document Number	Rev	
	Vegas SKL/KBL-U	A000	
Date:	Thursday, June 16, 2016	Sheet 98 of 105	

Vegas SKL/KBL-U

Rev
A00

PCH_JTAG_TMS test point
 XDP_TMS test point
 PCH_JTAG_TDI test point
 XDP_TDI test point
 XDP_TCLK test point
 XDP_TCK_JTAGX test point
 XDP_TDO_CPU test point
 PCH_JTAG_TDO test point



<Core Design>



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 Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU XDP;PCH XDP

Size

Document Number

Rev

Vegas SKL/KBL-U

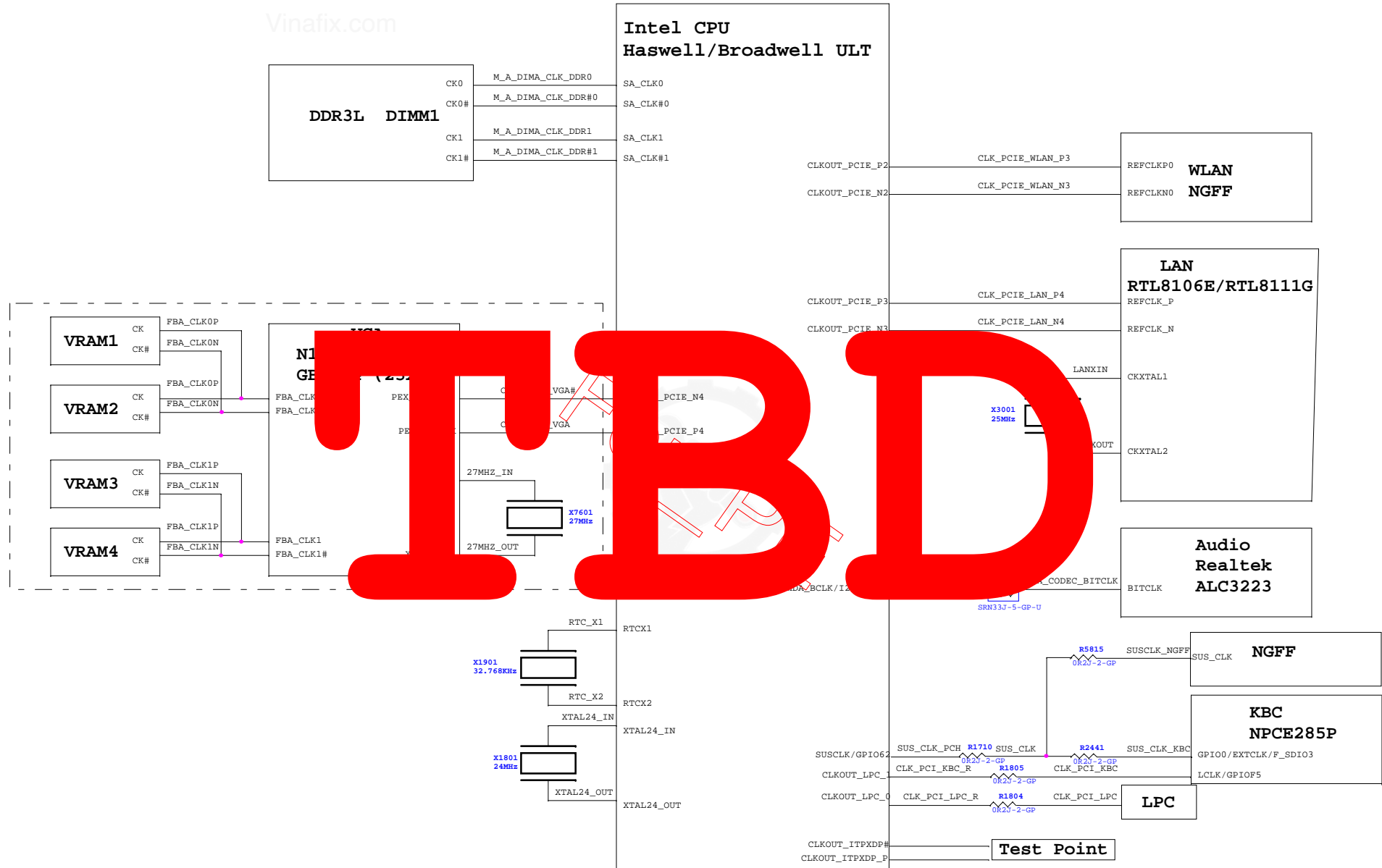
A00

Date: Thursday, June 16, 2016

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CLK Block Diagram

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Change notes -

[illegible]

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Title

Change History

Size
A3

Document Number

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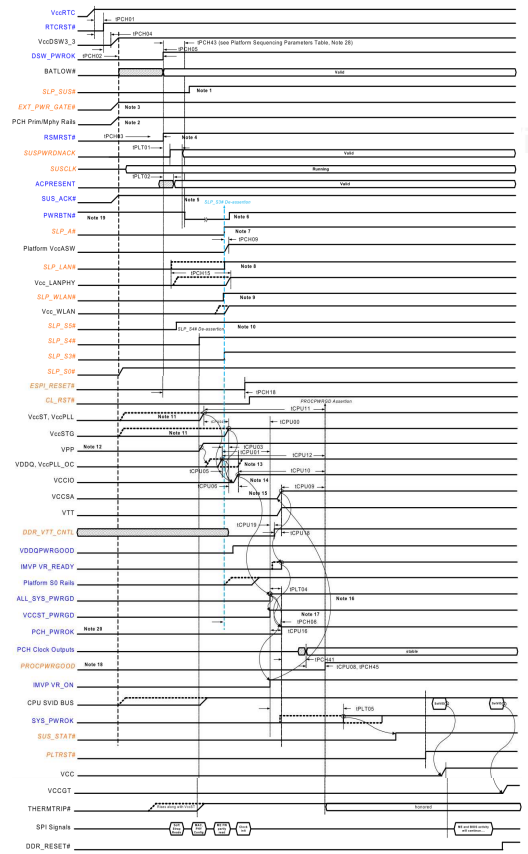
Rev

400

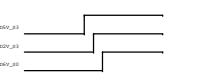
Date: Thursday, June 16, 2016

Sheet 101 of 105

SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



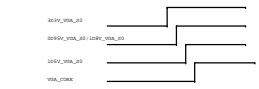
For DDR4 power sequence



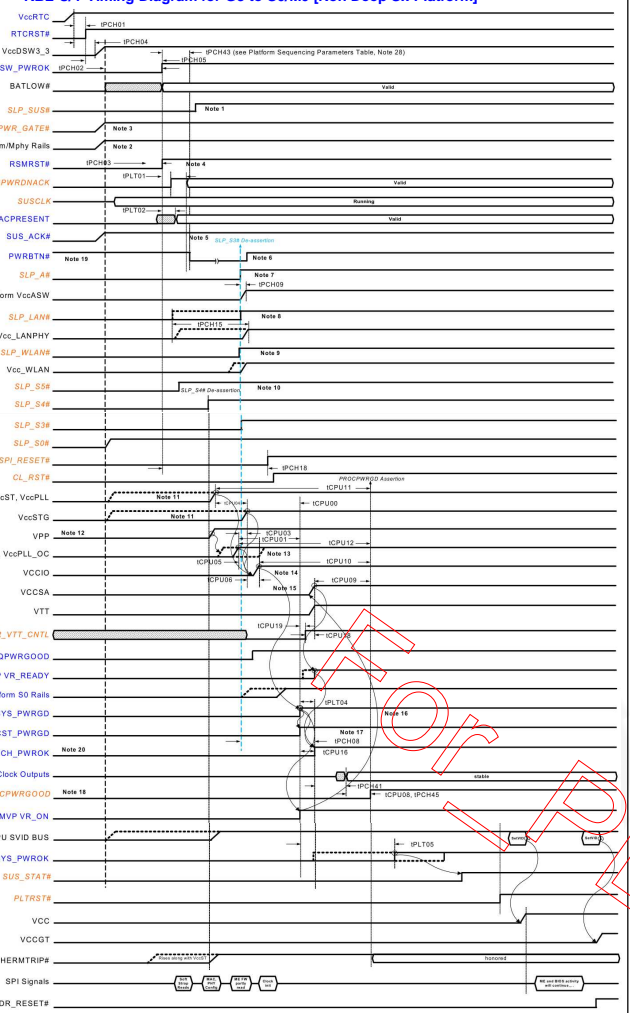
AMD GPU Power sequence

303V_VGA0
=> 0D95V_VGA_S0/1DSV_VGA_S0
=> 1DSV_VGA_S0
=> VGA_CORE

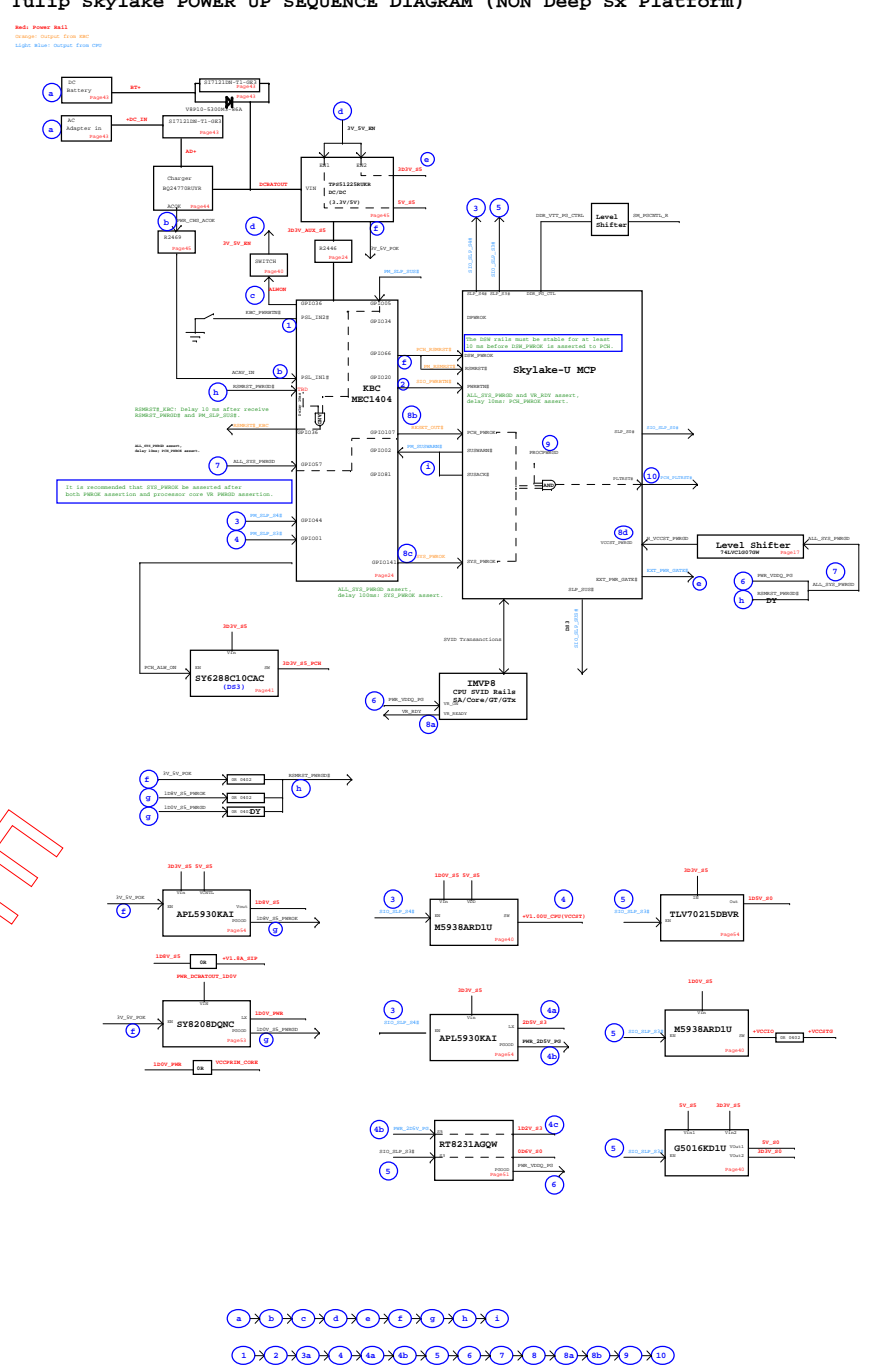
20ms
All the AGIC supplies must reach their respective nominal voltages within of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.
It is recommended that the 3.3V rail ramp up first.
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

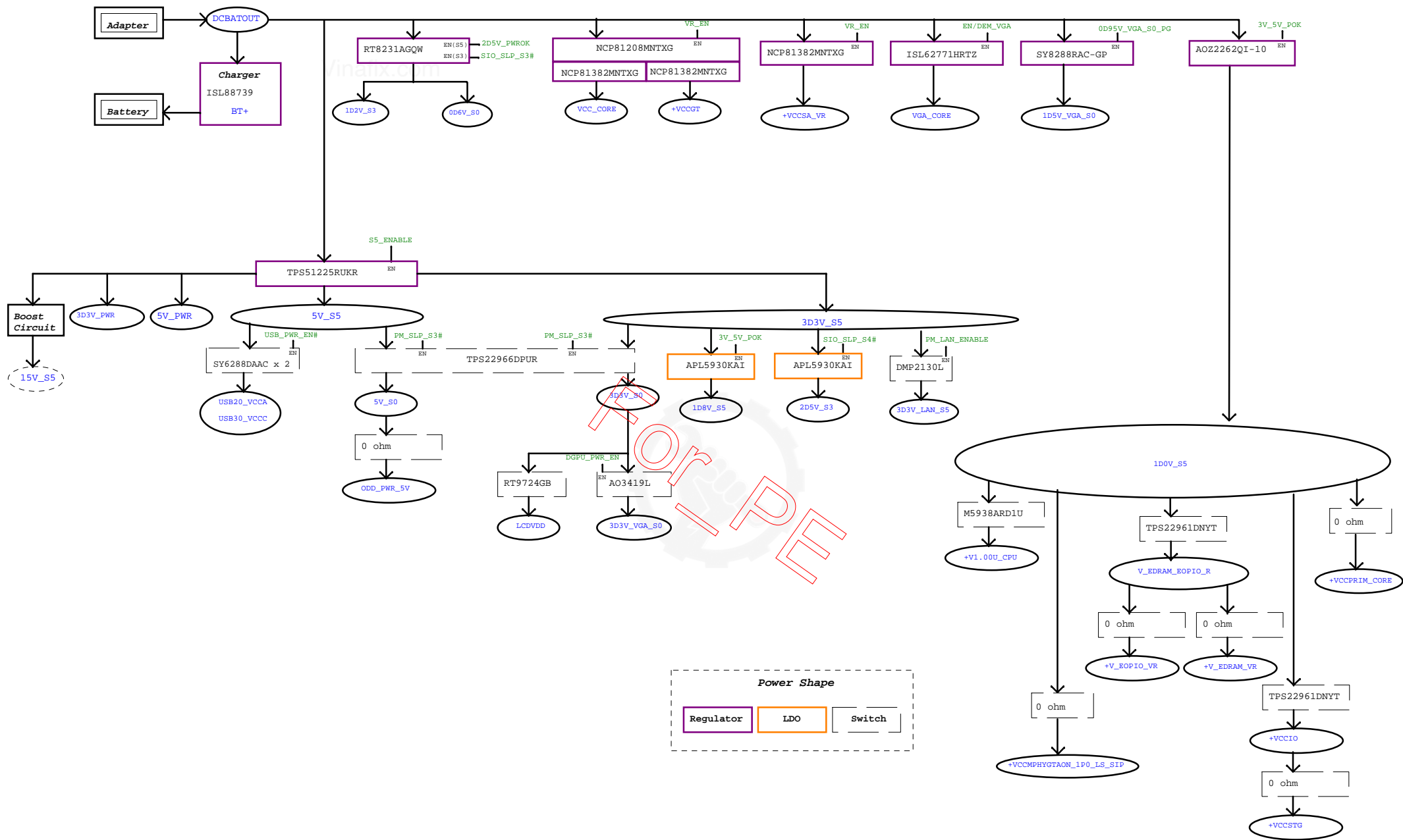


KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

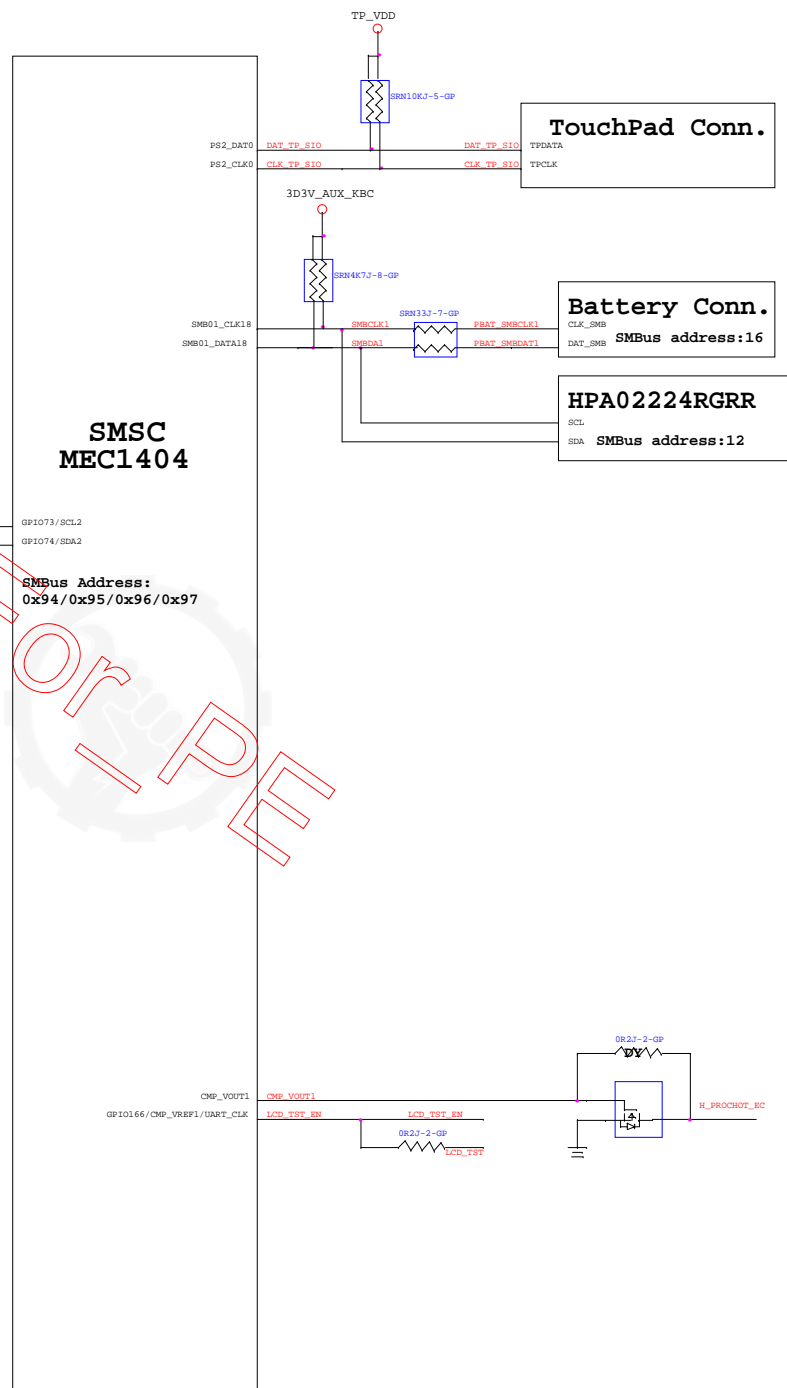


Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



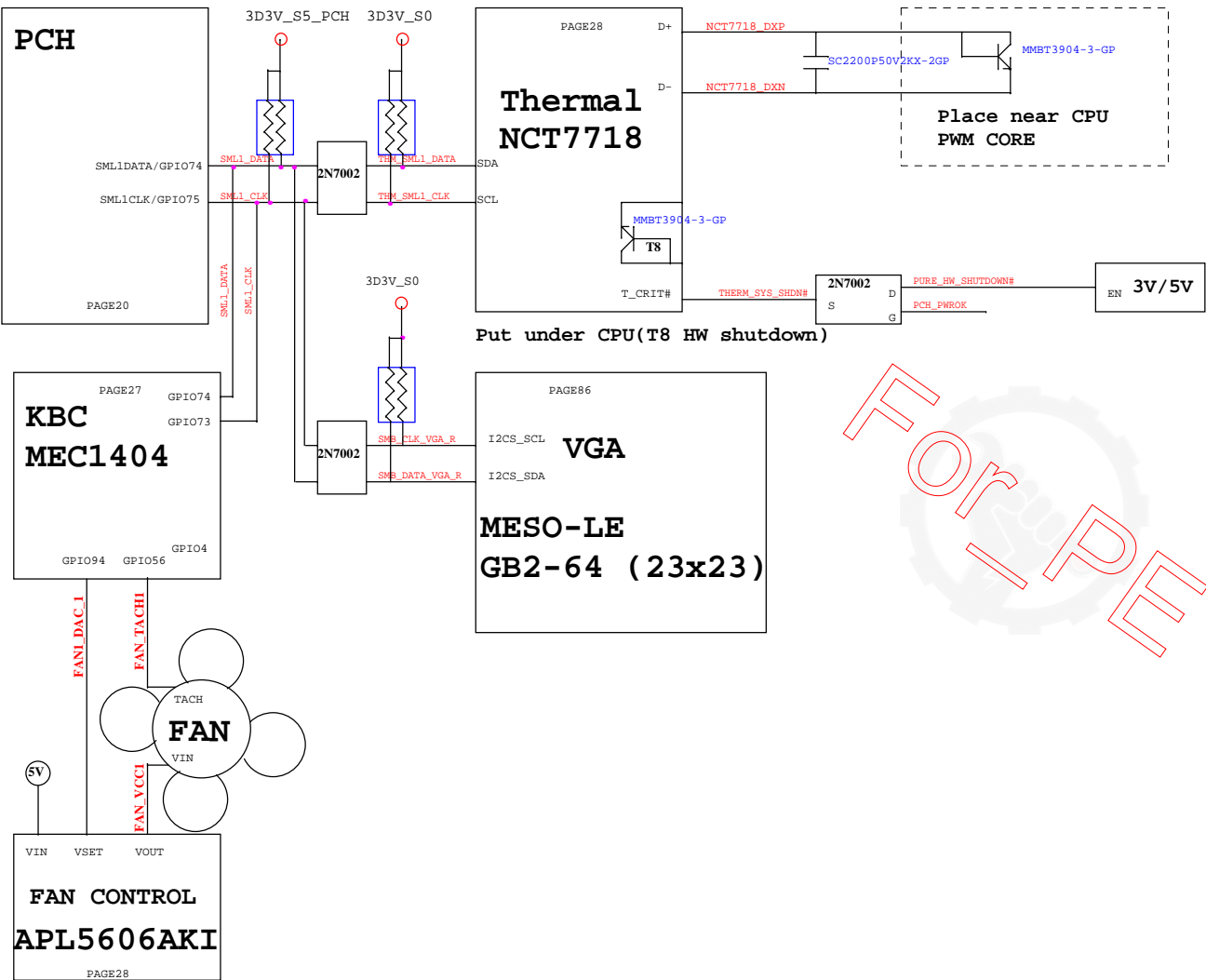


KBC SMBus Block Diagram



Thermal Block Diagram

Vinafix.com



Audio Block Diagram

